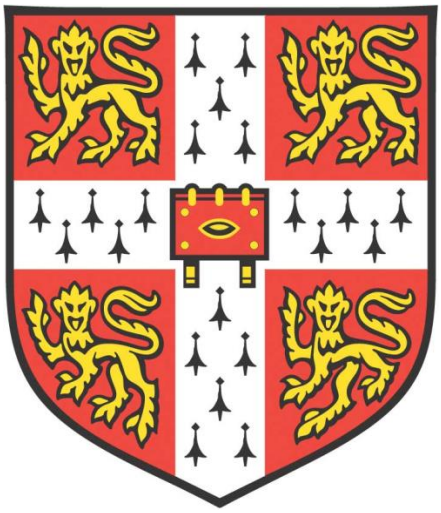
TWO-DIMENSIONAL ELECTRONICS: FROM MATERIAL SYNTHESIS TO DEVICE APPLICATIONS



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This dissertation is submitted for the degree of Doctor of Philosophy

November 2018

To my beloved husband and best friend,

Yu Ni

DECLARATION

This dissertation contains the research results performed by the author between October 2014 and July 2018 in the Department of Engineering, University of Cambridge. This dissertation is the result of my own work and includes nothing which is the outcome of work done in collaboration except as declared in the Preface and specified in the text. It is not substantially the same as any that I have submitted, or, is being concurrently submitted for a degree or diploma or other qualification at the University of Cambridge or any other University or similar institution except as declared in the Preface and specified in the text. I further state that no substantial part of my dissertation has already been submitted, or, is being concurrently submitted for any such degree, diploma or other qualification at the University of Cambridge or any other University or similar institution except as declared in the Preface and specified in the text.

In accordance with the Department of Engineering guidelines, this thesis contains 50050 words and 76 figures, which does not exceed the length limit (65,000 words and 150 figures).

Shan Zheng

Cambridge, November 2018

Signed: Shan Zheng

Date: 1 November 2018

ABSTRACT

Shan Zheng

Two-dimensional (2D) materials have attracted extensive research interest in recent years. Among them, graphene and the semiconducting transition metal dichalcogenides (TMDs) are considered as promising candidates for future device applications due to their unique atomic thickness and outstanding properties. The study on graphene and TMDs has demonstrated great potential to further push the scaling of devices into the sub-10 nanometer regime and enable endless opportunities of novel device architectures for the next generation.

In this thesis, crucial challenges facing 2D materials are investigated from material synthesis to electronic applications. A comprehensive review of the direct synthesis of graphene on arbitrary substrates with an emphasis on the metal-catalyst-free synthesis is given, followed by a detailed study of the contact engineering in TMDs with a focus on the strategies to lower the contact resistance. Effective approaches have been demonstrated to solve these issues. These include: (1) metal-catalyst-free synthesis of graphene on various insulating substrates; (2) Fermi level pinning observed in TMDs and integration of graphene contact to lower the contact resistance; and (3) application of metal-insulator-semiconductor (MIS) contact in TMD field-effect transistors (FETs).

First, a direct low-temperature synthesis of graphene on insulators without any metal catalysts has been realized. The effects of carbon sources, NH_3/H_2 concentrations, and insulating substrates on the material synthesis have been systematically investigated. Graphene transistors based on the as-grown material have been fabricated to study the electronic properties, which can further confirm the nitrogen-doped graphene has been synthesized from the electrical characterizations. Then electronic devices focusing on the semiconducting TMDs has been studied. The Fermi level pinning has been observed and studied in WS_2 FETs with four metal materials. A novel method of using graphene as an insertion layer between the metal and TMDs has been proven to effectively reduce the contact resistance. Owing to the benefit of tuning the graphene work function *via* the electric field, the contact resistance can further be reduced. Finally, the effectiveness of MIS contacts in WS_2 FETs has been demonstrated. A thickness dependence research has been conducted to find the optimal thickness of the inserted insulator. Moreover, the possible physical mechanism of how this MIS contact reduces the contact resistance in 2D materials has been discussed.

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LIST OF PUBLICATIONS

1. **Shan Zheng,** Guofang Zhong, Xingyi Wu, Lorenzo D'Arsiè, and John Robertson. "Metal-catalyst-free growth of graphene on insulating substrates by ammonia-assisted microwave plasma-enhanced chemical vapour deposition." *RSC Advances* 7.53 (2017): 33185-33193.
2. **Shan Zheng,** Yuzheng Guo, Xingyi Wu, Guofang Zhong, and John Robertson. "Contact resistance reduction in WS_2 field-effect transistors using a graphene insertion layer." *In submission*.
3. **Shan Zheng,** Dameng Liu, and John Robertson. "Insertion of an ultrathin Al_2O_3 interfacial layers for the Schottky barrier height reduction in WS_2 field-effect transistors." *In submission*.
4. Girish Rughoobur, Hisashi Sugime, Mario DeMiguel-Ramos, Teona Mirea, **Shan Zheng**, John Robertson, Enrique Iborra, and Andrew John Flewitt. "Carbon nanotube isolation layer enhancing in-liquid quality-factors of thin film bulk acoustic wave resonators for gravimetric sensing." *Sensors and Actuators B: Chemical* 261 (2018): 398-407.

Conference Presentations

1. **Shan Zheng (presenting author)**, Yuzheng Guo, Xingyi Wu, Guofang Zhong, and John Robertson. "Controllable Schottky barrier heights in graphene/WS_2 heterostructure transistors." *Materials Research Society Fall Meeting & Exhibit 2016*, Boston, United States.
2. Guofang Zhong, Xingyi Wu, **Shan Zheng (presenting author)**, Lorenzo D'Arsiè, Kenneth B. K. Teo, Nalin L. Rupesinghe, Alex Jouvray, and John Robertson. "Continuous graphene growth by open roll-to-roll chemical vapor deposition system." *31st International Winterschool on Electronic Properties of Novel Materials 2017*, Kirchberg/Tirol, Austria.

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LIST OF ABBREVIATIONS AND ACRONYMS

AFM	Atomic Force Microscope
ALD	Atomic Layer Deposition
APS	Ammonia Persulfate Solution
CBM	Conduction Band Minimum
CBO	Conduction Band Offset
CMOS	Complementary Metal-Oxide-Semiconductor
CNT	Carbon Nanotube
CNL	Charge Neutrality Level
CVD	Chemical Vapour Deposition
DC	Direct Current
DFT	Density Functional Theory
DI water	De-ionized water
EBL	Electron-Beam Lithography
FET	Field-Effect Transistor
FETT	Field-Effect Tunnelling Transistor
FWHM	Full Width at Half Maximum
h-BN	hexagonal-Boron Nitride
ICP	Inductively Coupled Plasma
IPA	Isopropyl Alcohol
MIS	Metal-Insulator-Semiconductor
MIGS	Metal Induced Gap States
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
OM	Optical Microscopy
PDMS	poly(dimethyl siloxane)
PECVD	Plasma-Enhanced Chemical Vapour Deposition
PMMA	poly(methyl methacrylate)
RF	Radio Frequency
RIE	Reactive Ion Etching
S/D	Source/Drain

SEM	Scanning Electron Microscope
STM	Scanning Tunnelling Microscopy
TMA	trimethylaluminum
TDMAH	tetrakis(dimethylamino)hafnium
TDMAT	tetrakis(dimethylamino)titanium
TMD	Transition Metal Dichalcogenides
VBM	Valence Band Maximum
VBO	Valence Band Offset
XPS	X-ray Photoemission Spectroscopy

LIST OF APPENDICES

1 INTRODUCTION

1.1 Motivation

Over the past few decades, the development of the semiconductor industry has followed Moore's Law by subsequent transistor downscaling for faster, cheaper, and more energy-efficient integrated circuits (ICs). However, as the feature size of silicon transistors is approaching the quantum limit, people are looking for new alternative materials and novel structure designs to further boost the performance and sustain such development. The two-dimensional (2D) layered material family has provided great opportunities owing to its atomic thickness and superior properties, making it a promising candidate for the replacement of channel materials, electrodes, dielectrics as well as the endless possibilities of van der Waal all-2D device structures.

The discovery of graphene has led the rapid increase of the research in 2D materials since 2004.[1] Its outstanding electrical, mechanical and thermal properties have been experimentally demonstrated,[2–4] so have the various applications including field-effect transistors (FETs), transparent conductive electronics, gas detectors, and biosensors.[5] To fulfil its unique properties, one of the most fundamental challenges is to develop a graphene synthesis method that can yield commercially viable graphene while mostly maintaining its record properties.

The commonly used methods for graphene synthesis involve mechanical exfoliation, epitaxial growth on SiC, liquid phase exfoliation, and metal-catalyzed chemical vapour deposition (CVD). Mechanical exfoliation can produce high-quality graphene for fundamental research but is infeasible for scaled-up applications due to its low yield. Epitaxial growth on SiC requires quite expensive single crystalline substrates,

which limits its further applications. Liquid phase exfoliation is suitable for the industrial mass production, but the quality is very low. Metal-catalyzed CVD is a large-scale and cost-effective mainstream method to produce large-area and high-quality graphene, which facilitates the integration of graphene into the booming electronics and optoelectronics. Although metal-catalyzed CVD has demonstrated its great advantage, its own limited issues cannot be ignored. In general, the CVD method for graphene synthesis requires metal catalysts, high temperature, post-transfer process or additional catalyst removal techniques to apply the grown graphene onto arbitrary substrates for the further device applications. Specifically, the high temperature affects its compatibility with the existing silicon technologies. The complicated post-transfer process inevitably results in winkles, folds, holes, and resist residues in graphene, which degrades its quality and properties. Therefore, the game-changing breakthroughs would be the development of synthesizing graphene on arbitrary substrates without any metal catalysts at low temperature. Unfortunately, the metal-catalyst-free synthesis of graphene on insulators encounters tremendous difficulties in reducing the defects, preventing the vertical growth manner, and realizing the low-temperature growth.

Besides graphene, semiconducting 2D materials such as transition metal dichalcogenides (TMDs) have attracted increasing attentions recently. They are much favored in device aspects with great potentials to replace conventional channel materials. Although graphene owns a much higher carrier mobility, the absence of bandgap in graphene limits its application in digital devices. In contrast, the sizable bandgap of TMDs guarantees the low off-state current for transistors, thus reducing the static power consumption in logic circuits while retaining a typical on/off ratio up to six orders of magnitudes and a moderate mobility around several to a hundred at room temperature.[6] These advantages make TMDs possible for a variety of electronic and optoelectronic applications such as FETs, ICs, sensors and energy applications.[7]

One of the toughest challenges facing TMD electronics is to obtain a low contact resistance. For traditional silicon metal-oxide-semiconductor field-effect transistors (MOSFETs), the low contact resistances at the source/drain (S/D) are achieved by heavy doping through ion implantation. As a result, a large current can be realized from metal electrodes to the semiconductor channel. However, this doping technique cannot be simply applied to TMDs due to the atomically thin thickness nature of TMDs, and up to now, there is still no well-developed and air-stable doping methods in TMDs. Therefore, the Schottky barrier height at the metal and semiconductor interface becomes

the main factor that determines the contact resistance. To make things even worse, Fermi level pinning effect widely exists in TMDs,[8] leading to a large Schottky barrier height and the ineffectiveness of tuning the Schottky barrier height *via* the change of metal work functions. Therefore, TMD FETs commonly exhibit a small on-current with a large contact resistance, which is unable to meet the requirement of contact resistance down to 0.1 kΩ·μm for industrial applications.

1.2 Thesis Outline

This thesis focuses on the direct synthesis and material characterization of graphene on insulating substrates and the electronic device aspects on TMDs specifically WS_2 to address the challenges mentioned in the Motivation.

Chapter 2 introduces the atomic structures and electronic properties of graphene and TMDs. I will review the CVD methods used in the direct synthesis of graphene on insulators including transfer-free and metal-catalyst-free methods. The contact engineering of TMD devices is also reviewed with an emphasis on the strategies to lower the contact resistance.

Chapter 3 describes the main experimental techniques used in my research. The setup of a home-made microwave plasma-enhanced chemical vapour deposition (PECVD) and a commercial atomic layer deposition (ALD) system is described in detail. The graphene transfer method using the wet Cu etching and the all-dry transfer of TMDs are illustrated. Device fabrication techniques and characterizations are presented.

Chapter 4 reports the metal-catalyst-free synthesis of uniform and continuous graphene on various insulating substrates by microwave PECVD. The effects of carbon sources, NH_3 concentrations, and insulating substrates are discussed in detail to seek for the optimized low-temperature growth of graphene with the lowest density of defects. Electrical characterizations including FETs and sheet resistances are measured as supplementary evidences of N-doped and continuous graphene.

Chapter 5 presents an effective approach of reducing the contact resistance in WS_2 FETs based on the metal/graphene hetero-contacts. The Fermi level pinning effect is experimentally observed in WS_2 FETs with the direct metal contacts of four different metals. With the insertion of graphene, the on-current, on/off ratio, and field-effect mobility of WS_2 FETs are enhanced. Both high work function metal and low work function metal are investigated in the metal/graphene contact to WS_2 to study the

shifting the Fermi level of graphene with the metal contact doping and the gate voltage changing.

Chapter 6 demonstrates another novel method to lower the contact resistance in WS_2 FETs by inserting an ultrathin Al_2O_3 interfacial layer between the metal and WS_2. The advantage of this MIS contact structure to obtain a low contact resistance is verified in 2D semiconductors. The insulator thickness dependence behaviour is first observed in WS_2 and an optimal insulator thickness in achieving the lowest contact resistance is obtained. The underlying mechanism of the reduction in the Schottky barrier height due to the inserted insulator is explained from both the metal induced gap states (MIGS) theory and the dipole formation theory.

Chapter 7 summarizes the results and contributions of this thesis. A concluding overview of the values and limitations of this work is presented along with an outlook for future research.

2 BASIS OF 2D MATERIALS AND DEVICES

2.1 Graphene

Graphene is the name given to a 2D sheet of sp^2-hybridized carbon. Its extended honeycomb network is the basic building block of other important allotropes such as zero-dimensional (0D) fullerenes, one-dimensional (1D) carbon nanotubes (CNTs), and three-dimensional (3D) graphite (Figure 2-1).[9] It has supreme properties, such as mechanical stiffness, strength and elasticity, high electrical and thermal conductivity, and high carrier mobility,[10,11] making graphene as one of the most promising candidates to replace conventional materials in electronic and optoelectronic applications.

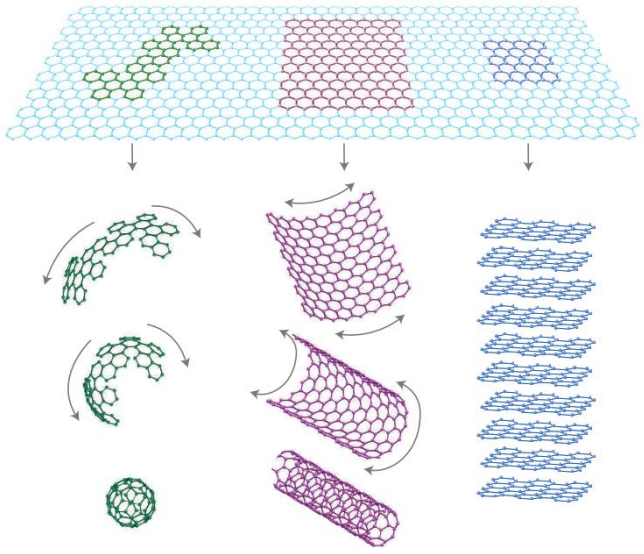

Figure 2-1 Graphene is a 2D building material for carbon materials of all other dimensionalities. ***Figure from Geim et al.***[10]

2.1.1 Atomic Structure of Graphene

The unit cell of graphene consists of two C atoms, arranged in a hexagonal honeycomb lattice as shown in Figure 2-2. The two atoms in the unit cell form the equivalent sub-lattices A and B. The two lattice vectors a_1 and a_2 can be written as[12]

$$a_1 = \frac{a_{C-C}}{2}\begin{pmatrix} 3 \\ \sqrt{3} \end{pmatrix}, a_2 = \frac{a_{C-C}}{2}\begin{pmatrix} 3 \\ -\sqrt{3} \end{pmatrix} \tag{2-1}$$

where a_{C-C} denotes the carbon-carbon bond length and is about 1.42 Å.[12] The lattice constant of graphene is about 2.461 Å by theoretical calculations.[13] The reciprocal-lattice vectors are given by[12]

$$b_1 = \frac{2\pi}{3a_{C-C}}\begin{pmatrix} 1 \\ \sqrt{3} \end{pmatrix}, b_2 = \frac{2\pi}{3a_{C-C}}\begin{pmatrix} 1 \\ -\sqrt{3} \end{pmatrix} \tag{2-2}$$

Of particular importance for the physics of graphene are the two points K and K' at the corners of the graphene Brillouin zone. These points are named Dirac points. Their position in momentum space are given by[12]

$$K = \left(\frac{2\pi}{3a_{C-C}}, \frac{2\pi}{3\sqrt{3}a_{C-C}} \right), K' = \left(\frac{2\pi}{3a_{C-C}}, -\frac{2\pi}{3\sqrt{3}a_{C-C}} \right) \tag{2-3}$$

The position of the three nearest-neighbor carbon atoms are given by the vectors[12]

$$\delta_1 = \frac{a_{C-C}}{2}\begin{pmatrix} 1 \\ \sqrt{3} \end{pmatrix}, \delta_2 = \frac{a_{C-C}}{2}\begin{pmatrix} 1 \\ -\sqrt{3} \end{pmatrix}, \delta_1 = -a_{C-C}\begin{pmatrix} 1 \\ 0 \end{pmatrix} \tag{2-4}$$

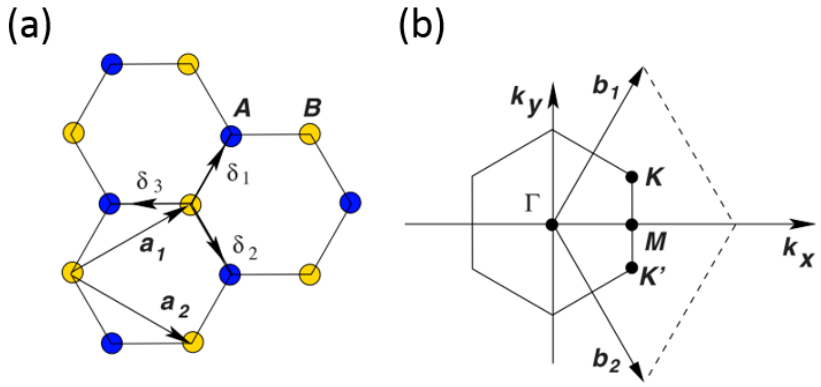

Figure 2-2 (a) Honeycomb lattice structure of graphene, which is made out of two interpenetrating triangular lattices (a_1 and a_2 are the lattice unit vectors, and $\delta_i, i = 1,2,3$ are the nearest-neighbour vectors). (b) The Dirac cones are located at K and K' points. *Figure from Neto et al.*[12]

In a perfect graphene sheet, all carbon atoms are sp^2-hybridized, with three in-plane σ-orbitals and two out-of-plane π-orbitals, as Figure 2-3 shows. This implies that each carbon atom can form equivalent σ-bonds to each of its three neighbouring atoms. The bonding energy of one C-C bond in graphene is about 4.93 eV.[14]

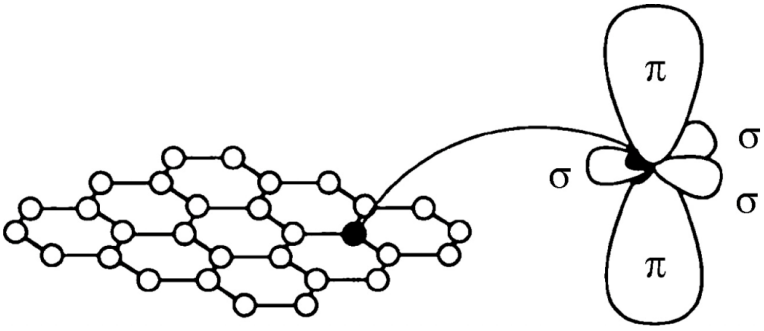

Figure 2-3 Structure of the sp^2 hybridization with three sp^2- (or σ-) orbitals and two p- (or π-) orbitals in the sp^2 honeycomb lattice. *Figure from Ado et al.*[15]

2.1.2 Electronic Properties of Graphene

Most properties of graphene are related to its electronic band structure, as plotted in Figure 2-4. In general, the energy bands of graphene can be given by[16]

$$E_{\pm}(k) = \pm t\sqrt{3 + f(k)} - t' f(k) \tag{2-5}$$

where

$$f(k) = 2\cos\left(\sqrt{3}k_y a_{c-c}\right) + 4\cos\left(\frac{\sqrt{3}}{2}k_y a_{c-c}\right)\cos\left(\frac{3}{2}k_x a_{c-c}\right) \tag{2-6}$$

the parameter k is the wave vector, t (≈2.8 eV) is the nearest-neighbour hopping energy (hopping between different sublattices), and t' is the next nearest-neighbour hopping energy (hopping in the same sublattice).[12] It is clear that the spectrum is symmetric around zero energy if $t' = 0$. For finite value of t', the electron-hole symmetry is broken and the π and π* bands become asymmetric. The plus sign applies to the upper π*–band, and the minus sign to the lower π–band.[12] The energy dispersion close to the Dirac points (K and K') can be approximated as the linear relationship with the momentum (q) relative to the Dirac points, being described by[16]

$$E_{\pm}(q) \approx \pm v_F |q| + \mathrm{O}\left[(q/K)^2\right] \tag{2-7}$$

where v_F is the Fermi velocity with its value of $v_F \approx c/300$ (where c is the velocity of light in vacuum).[17] Such a linear dispersion relation contrasts with the conventional parabolic dispersion of most semiconductor, $E(q) = q^2/2m$. The Fermi velocity in graphene does not change with energy or momentum, while in usual case, $v = k/m = \sqrt{2E/m}$ and hence the Fermi velocity changes substantially with energy. Actually, that linear relation resembles that of a photon $E = hck$, implying that close to the Dirac points, electrons and holes behave as massless charge carriers with a corresponding calculated Fermi velocity $v_F \approx (1.02\pm0.01)\times10^6$ m/s and a charge carrier mobility can be up to 250,000 cm^2/Vs.[18] The highest measured mobility values exceed 40,000 cm^2/Vs, even at room temperature and under ambient conditions.[19] This explains the extraordinary high mobility values predicted and detected in graphene and making graphene one of the promising materials for future electronic applications.

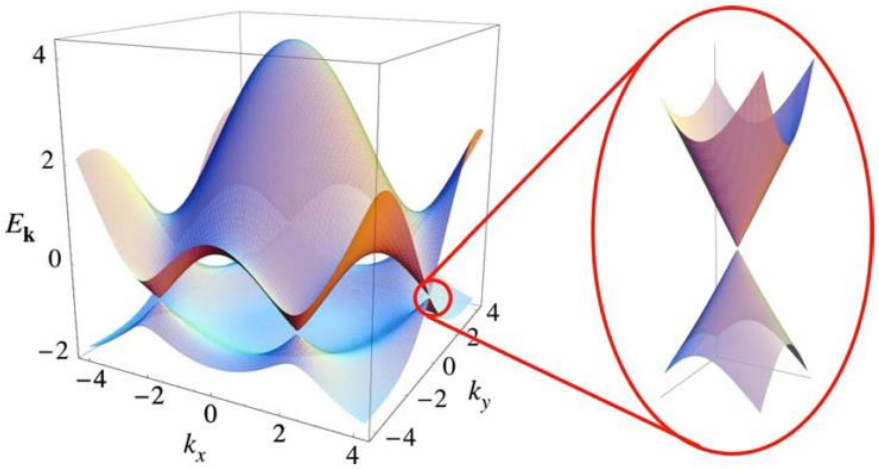

Figure 2-4 Three-dimensional representation of the π and π' electronic band structure with a zoom-in of the energy bands close to one of the Dirac points. *Figure from Neto et al.*[12]

2.2 Direct Synthesis of Graphene on Insulators

Graphene can be synthesized by mechanical exfoliation of graphite,[1] epitaxial growth on SiC surface,[20–22] liquid phase exfoliation,[23,24] and CVD. Among all the methods, CVD has become the most promising one due to its low cost, ability to produce high-quality and large-area graphene films and transfer onto desired substrates, and the compatibility with the current industrial-scale technologies.[25,26]

Graphene growth has been demonstrated on a variety of transition metal substrates such as Ni,[27–31] Cu,[32–34] Pt,[35] Fe,[36,37] Ir[38], Ru,[39,40] and Co.[41] During the reaction, the metal substrate not only works as a catalyst to lower the energy barrier of the reaction, but also determines the graphene deposition mechanism due to the different catalytic activity and solubility, which ultimately affect the quality of graphene.[42] The most commonly used metals are Ni and Cu, and the growth kinetics of graphene on these two metals are shown in Figure 2-5. The CVD of graphene on Ni proceeds *via* surface carbon segregation followed by precipitation process, due to the high carbon solubility of Ni (> 0.6 weight % at ~ 1326°C).[43] While the growth on Cu is a surface adsorption process other than carbon precipitation due to the low solubility of C atoms in Cu (< 0.001 ~ 0.008 weight % at ~ 1084°C),[43] which is known as a self-limiting surface reaction process. The remaining challenges facing the CVD graphene method on metals are to obtain a precise control over film thickness for various applications and optimize the transfer process to minimize its damage to graphene. However, the game-changing breakthroughs would be the development of growing graphene directly on arbitrary surfaces and/or at low temperature with fewer defects.[44]

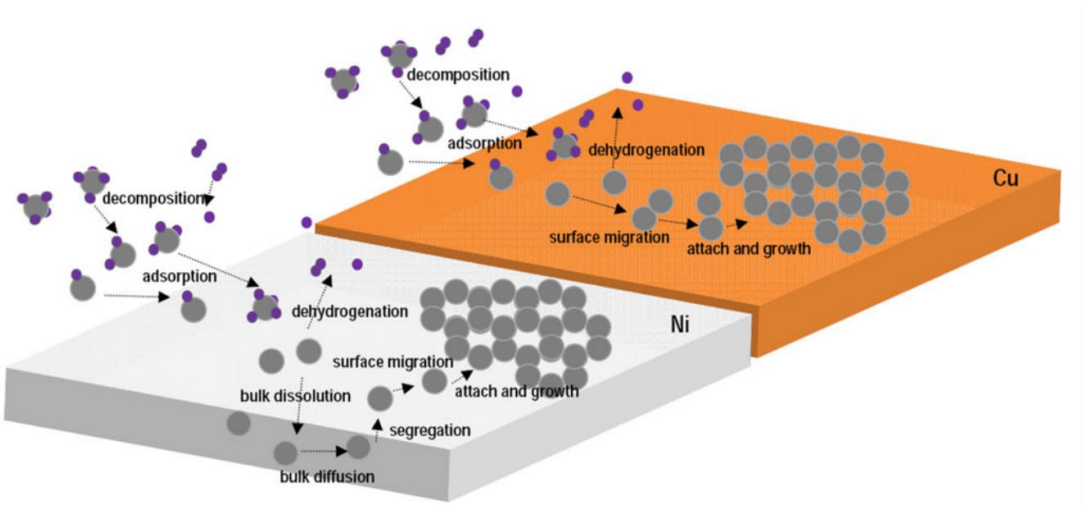

Figure 2-5 Growth kinetics in graphene formation steps on Ni and Cu. ***Figure from Muñoz et al.***[45]

2.2.1 Transfer-Free Synthesis

Although high-quality graphene can be synthesized on metals, the transfer process from metals onto arbitrary substrates is a critical step in the use of the CVD-grown graphene for most practical applications. However, the degradation of quality often occurs during the transfer process due to the tearing and ripping of graphene sheets, and

inevitable polymer and metal residues.[46] Therefore, it is very important to develop the transfer-free synthesis of graphene on arbitrary substrates to avoid all the problems that might be caused by the transfer process. Two transfer-free methods are mainly used, including synthesis *via* a sacrificial metal and by remote catalysation.

2.2.1.1 Sacrificial Metal Method

In the sacrificial metal method, the core idea is to use the catalytic effect of metals like Cu or Ni to act as media to directly grow graphene on insulating substrates. Then the mediated metal will be removed by chemical etching process. Gaseous carbon sources and solid carbon sources are both discussed in this method.

Gaseous carbon source is very suitable to grow large-area graphene sheets. Ismach *et al.*[47] first reported a novel transfer-free method to synthesize graphene using a sacrificial Cu layer at 1000°C, as Figure 2-6 shows. Monolayer graphene was formed through surface catalytic decomposition of hydrocarbon precursors on thin copper films pre-deposited on the quartz substrates. The copper films de-wetted and evaporated during or immediately after graphene growth, resulting in graphene grown directly on the bare quartz substrates. The growth temperature was reduced to 900°C by a continuous and wafer scale growth of multilayer graphene,[48] and can be further reduced to 600°C using a rapid-heating plasma chemical vapour deposition (RH-CVD).[49]

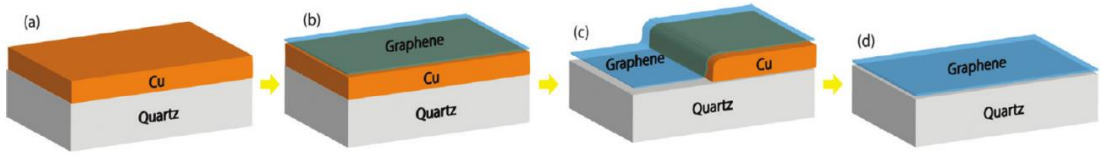

Figure 2-6 Schematic illustration of the graphene growth by a sacrificial Cu layer. (a) First a thin layer of copper is evaporated on the dielectric surface. (b) During the CVD using a mixture of H_2 and CH_4. (c) The metal de-wets and evaporates. (d) Leave the graphene layer on the substrate. *Figure from Ismach et al.*[47]

Solid carbon sources can be very effective and simple for developing a patterned structure and selective-area growth of graphene. Many solid carbon sources have been investigated, including SiC as the first trial,[50] followed by amorphous carbon,[51] graphite powder,[52] poly(methyl-methacrylate) (PMMA),[53,54] acrylonitrile-butadiene-styrene (ABS),[53,54] poly(2-phenylpropyl)methysiloxane (PPMS),[53] high-impact polystyrene (HIPS),[54] polycyclic aromatic hydrocarbons (PAHs),[55] and polyvinyl alcohol (PVA).[56]

The growth method varies from rapid thermal process (RTP) to normal thermal annealing. A typical growth process is illustrated in Figure 2-7.

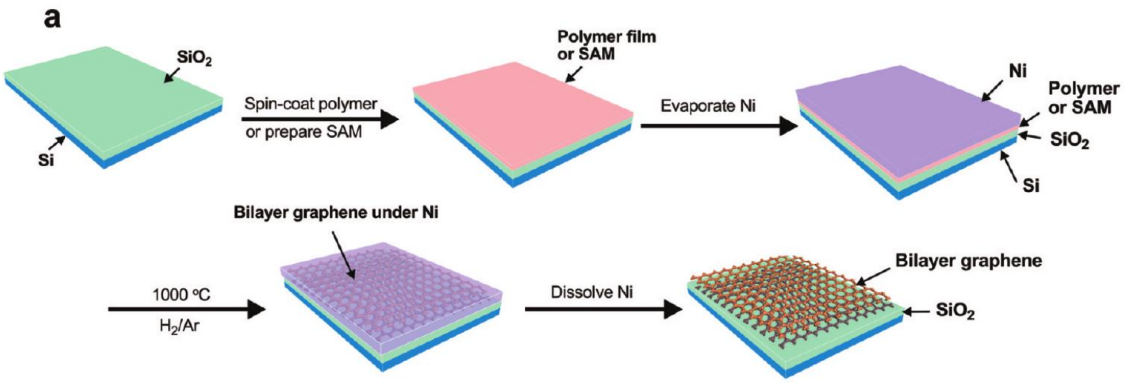

Figure 2-7 Schematic illustration of the graphene growth a sacrificial Ni layer. Bilayer graphene was derived from solid carbon sources (polymers or SAMs) on SiO_2/Si substrates by annealing the sample in an H_2/Ar atmosphere at 1000°C for 15 min. *Figure from Yan et al.*[53]

2.2.1.2 Remote Catalysation Method

The remote catalysation method is a novel approach to avoid the metal etching process which is necessarily needed in the sacrificial metal method. Instead of depositing metal on the substrate, the metal foil is placed near the substrate, leading to less metal contaminations and better uniformity in graphene.

Teng *et al.*[57] first reported the remote catalysation method for a direct growth of graphene layers on SiO_2 substrates. The floating gaseous metal atoms sublime from the metal foil and flow with the H atoms to decompose the carbon source (Figure 2-8). This method was further developed to improve the quality of the graphene films and reduce the growth temperature using a two-temperature reactor CVD system (1050°C + 800°C).[58] Recent developments of this method include changing the carbon source to amorphous carbon,[59] replacing Cu with Ga vapour catalyst,[60] and studying the size dependence on compressive strain.[61]

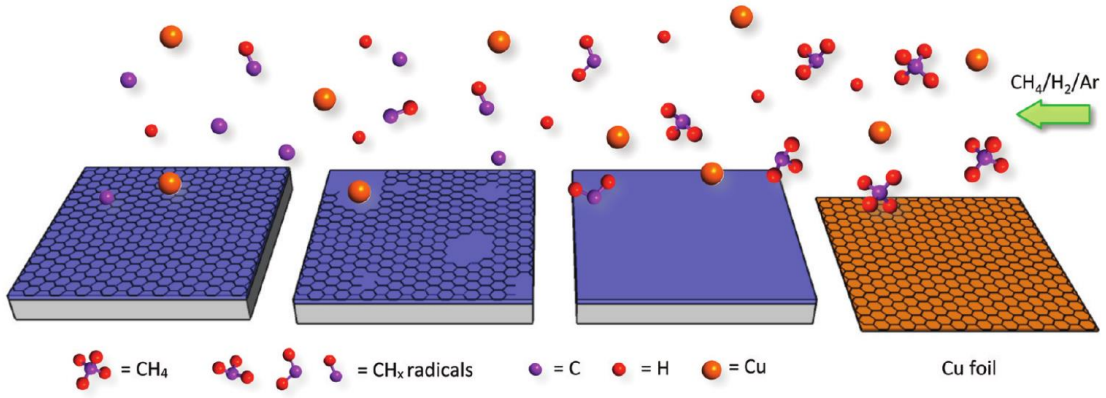

Figure 2-8 Schematic illustration of graphene growth mechanism involving decomposition of CH_4 by floating Cu and H. Cu particles are subliming from the Cu foil at 1000°C. Graphene starts growing on SiO_2 substrates after obtaining a certain distance from the Cu foil. ***Figure from Teng et al.*** [57]

2.2.2 Metal-Catalyst-Free Synthesis

It is widely believed that the presence of metals is indispensable for synthesizing high-quality graphene, since most CVD methods reported to date depend on the metal-catalyst growth. It requires costly metal substrates, metal catalyst removal procedures, and skilled transfer techniques to desired insulating substrates, so that the as-grown graphene could be ready to use in practical applications. However, the complex process usually results in metal contamination, wrinkling and breakage of graphene samples, and loss of metals.[26,62] Hence, it is of great significance to study the metal-catalyst-free growth of graphene on insulating substrates.

Nevertheless, due to the weak catalytic nature of insulators, there is no driving force for the decomposition of the carbon source, the nucleation, and growth of graphene. Therefore, the graphene grown directly on insulators faces many challenging issues such as repeated nucleation, high defects, slow growth rate, and small crystalline grain size. I will introduce how researchers tackled these challenges from two widely used methods, thermal CVD and plasma-enhanced CVD.

2.2.2.1 Thermal CVD

Thermal CVD is the most commonly used technique for the growth of graphene. Many attempts have been made to explore the metal-catalyst-free growth of graphene on various substrates including SiO_2,[63–67] Al_2O_3,[68–73] Ge,[74,75] Si_3N_4,[76,77] MgO,[78–80] $SrTiO_3$,[81] HfO_2,[82] TiO_2,[83] and h-BN.[84–87] Two-stage methods were proposed to improve the quality of graphene from two aspects: (1) dissociation of methane stage at a high-

temperature zone and graphene synthesis stage at a low-temperature zone;[64] or (2) nucleation stage at a high CH_4/H_2 ratio and growth stage at a low CH_4/H_2 ratio to avoid repeated nucleation.[76] Figure 2-9 illustrates a widely used thermal CVD system for graphene synthesis.

Despite all the efforts, the as-grown graphene on insulating substrates shares some common features of nanocrystalline and numerous grain boundaries, and high temperature is required due to the weak catalytic nature of insulators. Most experiments were carried out above 1000°C, and even as high as 1600 ~ 1650°C,[68,69] implying that high temperature is necessary for the metal-catalyst-free thermal CVD method. Only a few groups realized the growth below 1000°C, including one on α-Al_2O_3 (950°C),[70] two on Ge (910°C,[74] 900 ~ 930°C[75]), and two on MgO (325°C).[78,79] Although for some of them, the temperature was reduced, the density of defect increased and the quality of graphene was degraded for most graphene grown below 1000°C. Only one work can balance the good quality and low temperature very well by using hydrogen-terminated Ge as the substrates.[75]

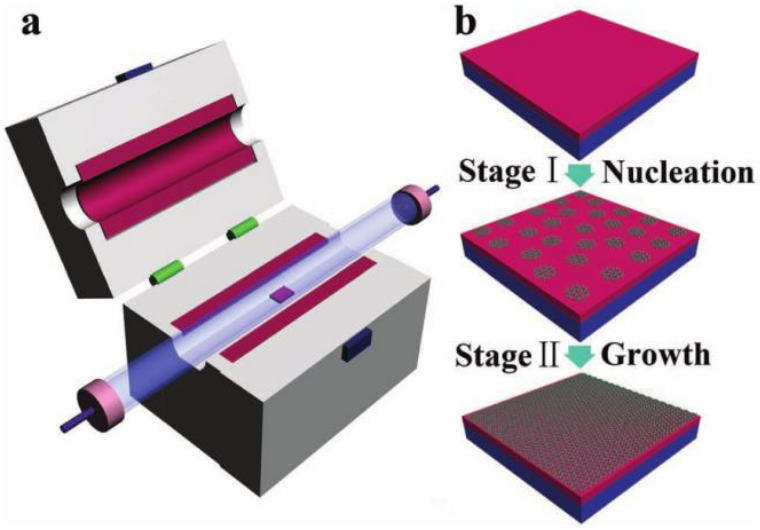

Figure 2-9 (a) Thermal CVD system. (b) Schematic diagram of the two-stage process for graphene synthesis. *Figure from Chen et al.*[76]

2.2.2.2 Plasma-Enhanced CVD

To overcome the high temperature needed in thermal CVD method, PECVD enables the graphene synthesis at low temperature with a better control in the film uniformity due to the presence of energetic and reactive species generated in the plasma region.

Several PECVD studies have been reported on SiO_2,[88–99] quartz,[88,91,94] glass,[97,100] and Al_2O_3[89,91] to explore the potential of PECVD for the metal-catalyst-free and low-temperature growth of graphene. Two-stage growth has been used in PECVD process to enlarge the isolated grain sizes,[88,89,92,93] and the growth temperature can be reduced to as low as 400˚C in a radiofrequency PECVE (RF-PECVD).[92] Nevertheless, extremely long growth times (over 9 hours)[88] or high-temperature pre-annealing (1000˚C)[92] was still needed, or only discontinuous films was produced.[89,92,93] Some attempts have been tried to synthesize continuous graphene using PECVD, however, these films suffered from common problems such as high density of defects, less surface uniformity,[90,91,94–100] and 3D nano-wall growth.[90,94,97,101]

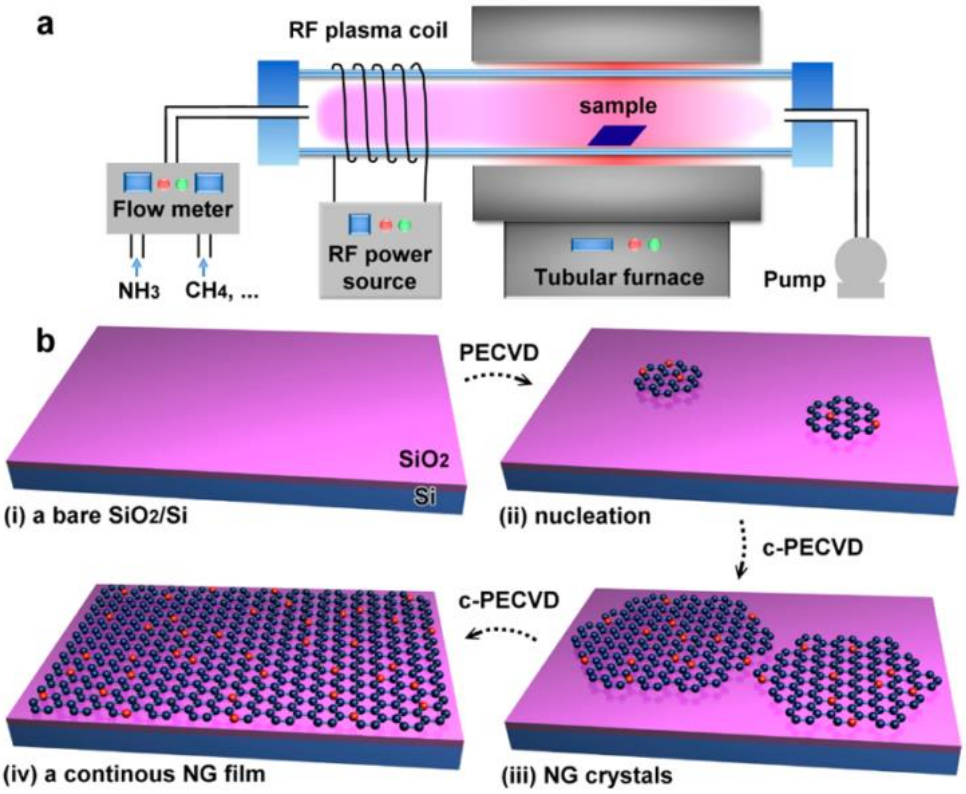

Figure 2-10 Schematic illustration of (a) the RF-PECVD system used for the growth of nitrogen doped graphene (NG) and (b) the growth procedure. *Figure from Wei et al.*[89]

2.2.3 Comparison of Methods

Among all the approaches, the transfer-free methods *via* a sacrificial metal or by remote catalysation can produce high-quality monolayer graphene with few defects, which can compete with those directly grown on metals. However, high temperature (800 ~ 1100°C) is normally required by transfer-free methods due to the use of metals

as catalysts, and the mobility (the largest one is 670 cm^2/Vs at room temperature) is not comparable to that of the metal-catalysed graphene. Moreover, this method cannot avoid the metal contamination problem and the quality of graphene would still be degraded.

As to the metal-catalyst-free thermal CVD method, it requires very high temperature (1100 ~ 1650°C) to produce good quality graphene. For the two works with high mobilities at room temperature, the required temperatures are 1650°C to achieve the mobility of 2000 cm^2/Vs, and 1570°C to achieve the mobility of 3000 cm^2/Vs. Moreover, all the graphene films with fewer defects were produced at relatively high temperature (above 1000°C).

When it comes to the metal-catalyst-free PECVD method, the growth temperature can be reduced to the range of 500 ~ 900°C with the aid of plasma. However, the density of defect has greatly increased at the same time. The high D peak observed in Raman spectroscopy reflects a common feature of the high density of defects in the graphene grown using plasma. Large numbers of domain boundaries and open edges of small crystallite sizes account for the strong D peak in the Raman spectrum. The representative methods for the direct synthesis of graphene have been summarized in Table 2-1.

In conclusion, the industrial-scale production of graphene is highly desirable to save energy consumption as well as the cost and increase the compatibility of graphene with modern silicon electronics technologies. It is still a big challenge to realize the direct growth of high-quality graphene on various insulating substrates at low temperature. Plenty of issues such as the metal contaminations, high density of defects, and high growth temperature need to be improved in the future.

Table 2-1 Comparison of methods for the direct synthesis of graphene

Ref	Method	Carbon source	Substrate	Temp °C	Time	μ cm^2/Vs	Domain size	Number of layer
Ref [47]	Sacrificial metal	CH_4	Cu	1000	7 h	NA	35 nm	Mono and multilayer
Ref [48]	Sacrificial metal	CH_4	Cu	900	5 min	670	NA	Multilayer

Ref [49]	Sacrificial metal	CH_4	Ni	900	1 min	43 ~580	12 ~ 20 µm	Monolayer
Ref [50]	Sacrificial metal-RTA	SiC	Ni	1100	30 s	NA	5 ~ 10 µm	Mono and multilayer
Ref [51]	Sacrificial metal-RTA	Amorphous C	Ni	1100	2 min	NA	NA	Monolayer
Ref [52]	Sacrificial metal-RTA	Graphite powder	Ni	25 ~160	5 min	667	5 ~ 20 µm	Mono and multilayer
Ref [53]	Sacrificial metal-RTA	Polymer or SAM	Ni	1000	20 min	110 ~220	NA	Bilayer
Ref [57]	Remote catalysation	CH_4	Cu	1000	30 min	100 ~600	Nano size	Multilayer
Ref [58]	Remote catalysation	CH_4	Cu	1050 +1000	30 min	1100	100 nm	Mono and multilayer
Ref [59]	Remote catalysation	Amorphous C	Cu	860	45 min	420	NA	Multilayer
Ref [63]	Thermal CVD	CH_4	SiO_2	1100 + 800	7 h	531	NA	Mono and multilayer
Ref [68]	Thermal CVD	CH_4	Sapphire	1425 ~1600	20 min	3000	32 ~ 270 nm	Mono and multilayer
Ref [70]	Thermal CVD	CH_4	Al_2O_3	950	2 h	277 ± 91	250 nm	Multilayer
Ref [75]	Thermal CVD	CH_4	Ge	900 ~930	30 min	2570 ±460	NA	Monolayer
Ref [78]	Thermal CVD	C_2H_2	MgO	325	1 h	NA	Nano size	Multilayer
Ref [81]	Thermal CVD	CH_4	$SrTiO_3$	1000	5 h	870~ 1050	250 nm	Mono and multilayer

Ref 88	PECVD	C_2H_2	Quartz	650	9 h	NA	500 nm	Mono and multilayer
Ref 89	PECVD	C_2H_2	SiO_2	650 ~700	90 min	100 ~400	300 nm	Monolayer
Ref 93	PECVD	CH_4	SiO_2	510 ~545	30 min	70	1.5 ~ 100 nm	Multilayer
Ref 94	PECVD	CH_4	SiO_2	650	20 min	NA	5 ~ 10 nm	Multilayer
Ref 96	PECVD	CH_4	SiO_2	500 ~900	4 h	105	100 nm	Multilayer

2.3 Transition Metal Dichalcogenides

TMDs are a family of 2D atomically thin materials. They have a common chemical formula of MX_2, where M represents the transition metal of groups 4-10, and X is the chalcogen atom (S, Se, or Te), as highlighted in Figure 2-11a. Note that TMDs from group 4 (Ti, Zr, or Hf), group 5 (V, Nb, or Ta), group 6 (Mo, W), or group 7 (Te, Re) are predominantly layered materials, whereas some TMDs of group 8-10 are commonly found in non-layered structures.[102] TMDs offer alternative solutions to compensate for graphene's weakness,[103] owing to the thinnest, air stable materials with sizeable energy bandgaps and high carrier mobilities, therefore TMDs become highly attractive for next-generation applications in electronics, optoelectronics, sensors and energy storage.[7] Beyond the reach of single material, there are endless possibilities of stacking various 2D materials to form multilayer van der Waals heterostructures like assembling atomic scale Lego (Figure 2-11b), which opens up appealing opportunities for designing novel device architectures with tunable electronic properties.

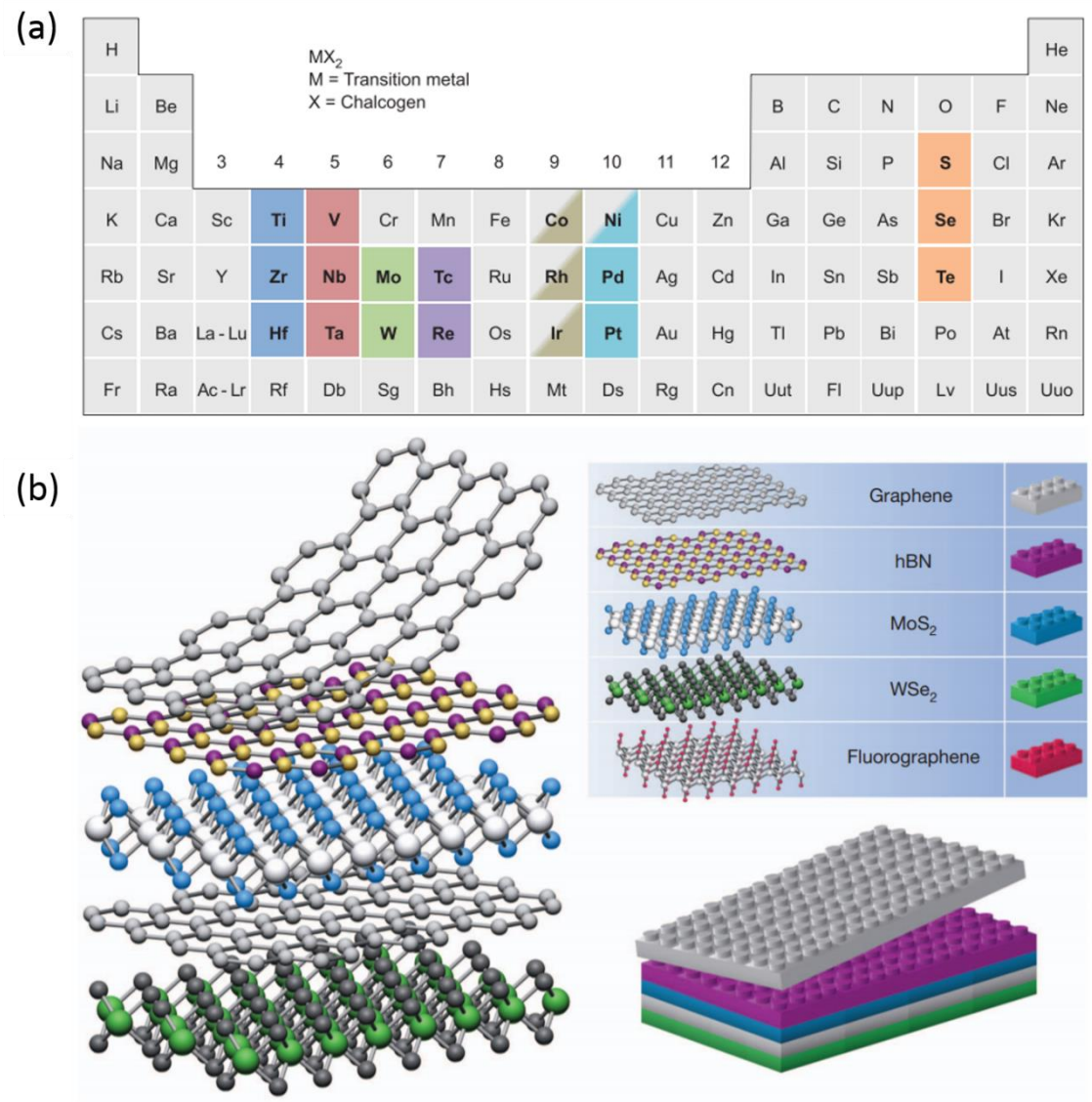

Figure 2-11 (a) Transition metals and three chalcogen elements highlighted in the periodic table. (b) Building van der Waals heterostructure if 2D crystals are analogous to Lego blocks. *Figures from Chhowalla et al.* [102] *and Geim et al.*[103]

2.3.1 Atomic Structure of TMDs

The layered structures of TMDs come from the stacking of an individual MX_2 monolayer, which contains trilayer atoms of sandwich units (X-M-X). Within each layer, the metal atom M is bonded to six chalcogen atoms X, with three above and three below arranged in configuration of either a trigonal prismatic (hexagonal, H) or octahedral (tetragonal, T) coordination, as shown in Figure 2-12. These sandwich units are then weakly bonded to each other through van der Waals forces to form the bulk crystal in various polytypes based on the stacking orders and metal atom coordination. In H-phase material, it is AbA stacking where the chalcogen atoms in two tetrahedrons

occupy the same position A in −z and +z direction, and the hexagonal symmetry can be observed from the top view (Figure 2-12a). While the T-phase corresponds to an AbC stacking sequence, where a trigonal chalcogen layer is on the top and 180-degree rotated structure (trigonal antiprismatic) is on the bottom (Figure 2-12b), and the hexagonal symmetry of chalcogen atoms can be seen from the top view.[7]

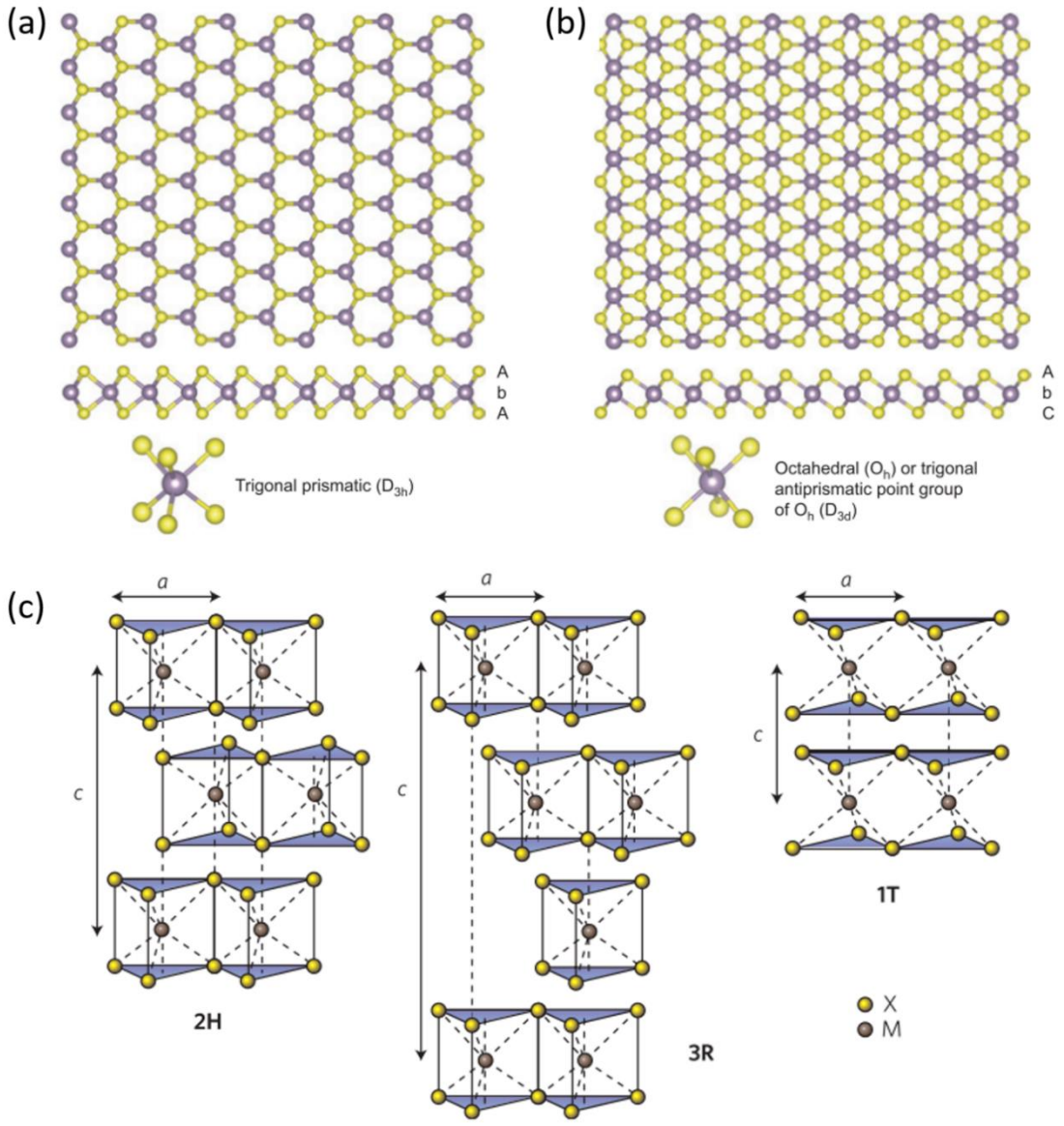

Figure 2-12 c-Axis and section view of monolayer TMDs with (a) trigonal prismatic (H) and (b) octahedral (T) coordination of metal atoms. (c) Schematics of arrangements of sandwich units for three typical phases (2H, 3R, 1T) of MoS_2 crystals. *Figures from Chhowalla et al.* [102] *and Wang et al.*[104]

Owing to the variation in polytypes, there is a wide range of electronic characteristics of TMDs ranging from insulator like HfS_2, to semiconductor like MoS_2 and WS_2, and semi-metals like $MoTe_2$ and WTe_2, to metals like NbS_2.[102] Even for the

same material, its structural phases can affect the electronic properties. Taking MoS_2 as an example, it has three different phases including 2H (hexagonal symmetry), 3R (rhombohedral symmetry), and 1T (tetragonal symmetry) as shown in Figure 2-12c. The 2H and 3R phases are semiconducting but the 1T phase is metallic, so the phase change can induce the property change, which can be used to reduce the contact resistance.[6]

2.3.1 Electronic Properties of TMDs

As discussed above, the various chemical compositions and structural phases of TMDs reveal a broad range of bandgaps covering from metals to insulators. Here, the band structure of the semiconducting TMDs formed by transition metal group 6 (Mo, W) combined with S and Se will be discussed. A common feature shared by these TMD semiconductors is the bandgap becomes wider with decreasing the atomic layers due to quantum confinement effects, and a transition from an indirect bandgap has been observed when the bulk materials are scaled down to monolayer.[102]

Figure 2-13 shows the band structures of MoS_2 with different thicknesses calculated by density functional theory (DFT).[105] The bulk, 4L, 2L MoS_2 are indirect gap semiconductors with smaller bandgaps, and the conduction band minimum (CBM) and the valence band maximum (VBM) are located at the Γ point and the midpoint between K and Γ respectively. In contrast, the monolayer MoS_2 exhibits a direct bandgap with VBM and CBM coinciding at the K point with a widening bandgap. The conduction band states at the K point remain roughly unchanged with the number of layers, because these states are caused by the localized *d* orbital of the metal Mo which is in the middle of the S-Mo-S unit with the minimum effect by the interlayer coupling. On the other hand, the states near the Γ point are caused by a linear combination of *d* orbitals of Mo atoms and antibonding p_z orbitals of the S atom, which results in a strong interlayer coupling. So, the interaction between any two layers is the same and these state energies are sensitively dependent on the number of layers while the monolayer lacks the interlayer interaction. This could explain the bandgap increases as the number of layers decreases from the bulk to the monolayer.

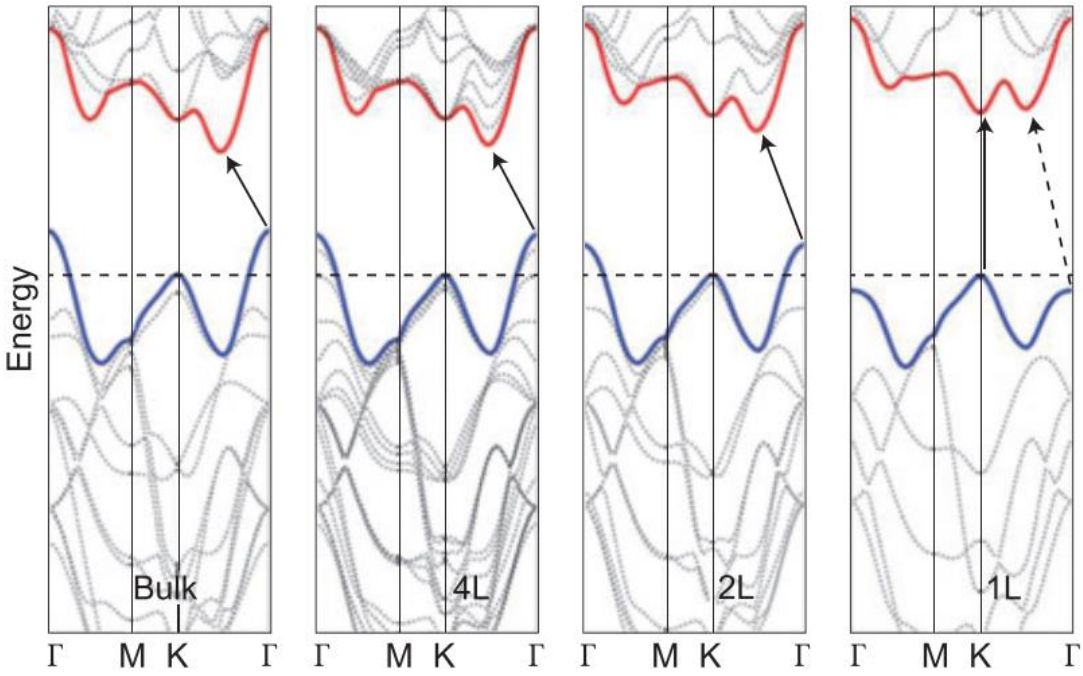

Figure 2-13 Energy dispersion in bulk, quadrilayer (4L), bilayer (2L), and monolayer (1L) MoS_2. *Figure from Splendiani et al.*[105]

The bandgaps in most TMDs are in the range of 1.01 ~ 2.0 eV in the bulk and 1.31 ~ 2.38 eV in the monolayer (Figure 2-14).[106] Specifically, the widely studied semiconducting TMDs like MoS_2, $MoSe_2$, WS_2, and WSe_2 have the bandgaps ranging from 1.09 ~ 1.57 eV in the bulk and 1.55 ~ 1.99 eV in the monolayer, which are comparable to that in silicon (1.1 eV).[104] Therefore, unlike the absence of a sizable bandgap in graphene that limits its application in digital electronic devices, the natural bandgap of TMDs enables their integration with current silicon technologies such as logical transistors as attractive channel materials and heterojunction applications based on the band engineering. Furthermore, the transition to a direct bandgap can be observed in photoluminescence spectroscopy. A strong photoluminescence indicates monolayer MoS_2, $MoSe_2$, WS_2, and WSe_2, while a weak or negligible photoluminescence can be seen in multilayer and bulk materials.[102] The strong photoluminescence and large exciton binding energy in a direct bandgap in the monolayer TMDs provide the fundamental basis for their practical applications in optoelectronics and sensors.[104]

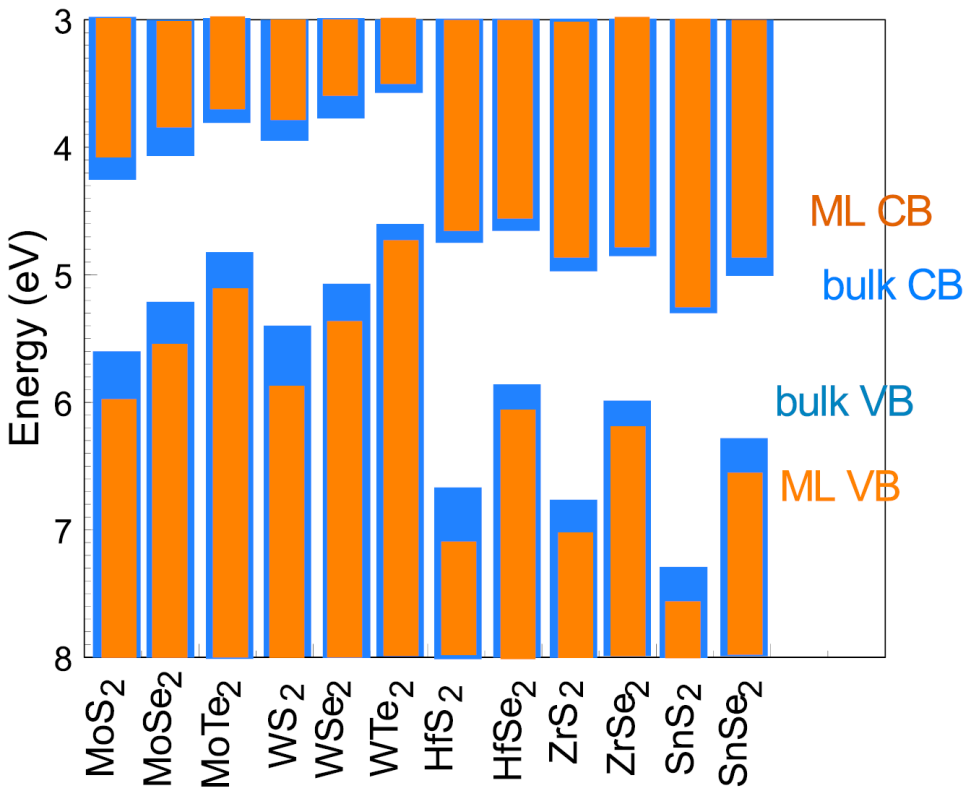

Figure 2-14 Summary of electron affinities and ionization potentials of various monolayer (ML) and bulk TMDs. ***Figure from Guo et al.***[106]

2.4 Contact Engineering for TMDs

The field of TMDs has received increasing attention with booming material choices and device architectures to improve the device performance and cost-efficiency. The most widely investigated electronic device in TMDs is FETs, and the contacts between bulk metal electrodes and the semiconducting TMD channel are very crucial communication links for the efficient integration of 2D TMDs to the 3D world. Therefore, a low contact resistance is highly required to obtain large on-current, large photoresponse and high-frequency operation.[107] However, the large contact resistance between 2D TMDs and bulk metals drastically restrains the drain current.[107] How to contact TMDs becomes a significant challenge facing the further development of TMD electronic and optoelectronic applications. Here, the origin of metal/TMD contacts and effective strategies to reduce the contact resistance will be reviewed.

2.4.1 Metal/TMD Contacts

According to the Schottky-Mott theory,[108] when a metal makes intimate contact with a semiconductor, the Fermi level in the two materials must be equal at thermal

equilibrium, and the vacuum level must be continuous, thus the two Fermi levels align so the semiconductor Fermi level at the interface is modified. The potential barrier Φ_{SB} between the two should ideally be set by the metal work function Φ_M and the semiconductor electron affinity χ, thus the metal/TMD contacts can be characterized by the Schottky barrier height expressed by

$$\Phi_{SB-n} = \Phi_M - \chi \qquad \Phi_{SB-p} = E_g - (\Phi_M - \chi) \tag{2-8}$$

where Φ_{SB-n} and Φ_{SB-p} are the Schottky barrier height for electron and hole injection, respectively, and E_g is the bandgap of the semiconductor. Low work function metals are normally used to effectively inject electrons to n-type semiconductors because of the Fermi level aligned close to the conduction band, while high work function metals are expected to contact p-type semiconductors to allow easier hole injection. However, this dependence is not experimentally observed, leading to the ineffectiveness of changing the metal work function to accordingly tune the Φ_{SB}, and this phenomenon is called Fermi level pinning. In reality, this pinning effect is taken into consideration to calculate the Φ_{SB}. If the semiconductor interface state energy comes from the MIGS, the charge neutrality level (E_{CNL}) is up to which of the MIGS are filled at a neutral state. The accurate Φ_{SB} is found to follow a linear dependence on an effective metal work function $\Phi_{M.eff}$ other than the normally referenced metal work function in vacuum Φ_M. The equations are shown below:[109]

$$\begin{aligned} \Phi_{M.eff} &= S\Phi_M + (1-S)E_{CNL} \\ \Phi_{SB} &= \Phi_{M.eff} - \chi \end{aligned} \tag{2-9}$$

Here the slope $S = d\Phi_{SB} / d\Phi_M$ is the pinning factor and varies between the strongly pinned limit of $S_{\min} = 0$ (Bardeen limit) and the weakly pinned limit of $S_{\max} = 1$ (Schottky limit). So less pinning effect means it would be much easier to modulate the Schottky barrier height *via* the change of metal work functions and the range of the barrier that can be adjusted by metals would be relatively large.

Figure 2-15 shows the calculated band alignment *via* DFT for a variety of TMDs in both multilayer and monolayer to form a contact with the most commonly used metals with different work functions.[106,110] Taking MoS_2 for example, the slope S is calculated to be 0.28 for monolayer and 0.33 for multilayer case.[111] Experimentally, the slope S is fitted to be ~ 0.1,[112–115] implying a strong Fermi level pinning at the metal/MoS_2 interface. The experimental value is lower than the simulation one, and the possible

reason could be the extra pinning added due to the inevitable creation of defects when fabricating the contact.[111] In the case of WS_2 and WSe_2, both experiments[116,117] and simulations[111,118] indicate that the pinning level is closer to the middle of the bandgap, making it even more difficult to obtain a low contact resistance.

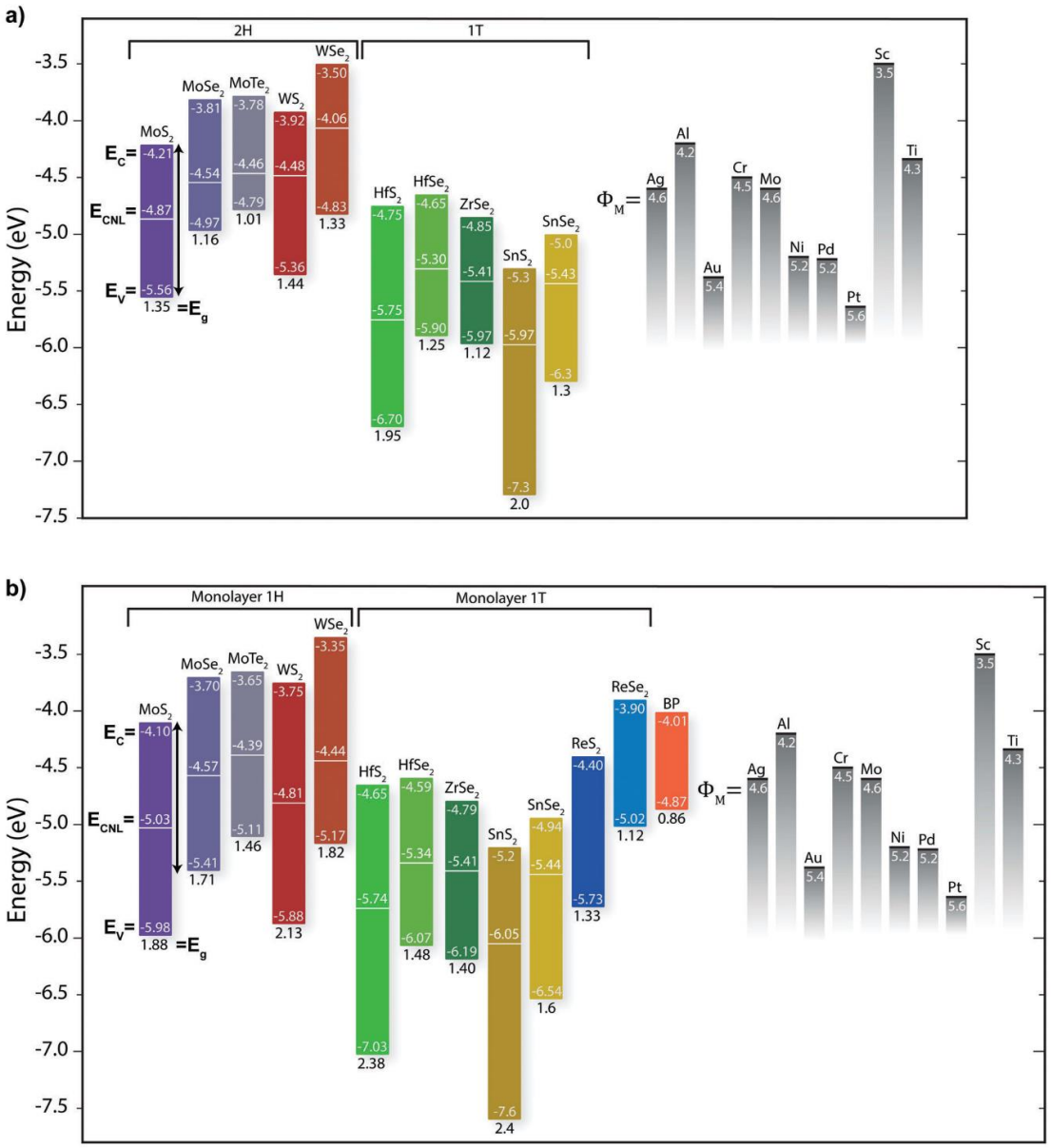

Figure 2-15 Schematic band alignment of various TMD/metal contacts for (a) multilayer and (b) monolayer situation. Important values are labelled in the graph including bandgap (E_g), electron affinity, ionization potential, charge neutrality level (E_{CNL}), and the work functions Φ_M of commonly used metals. *Figure from Schulman et al.*[8]

2.4.2 Origin of Fermi Level Pinning

There is still no consensus on the origin of the Fermi level pinning in metal/TMD contacts and numerous assumptions and conjectures are presented in active discussions. Some groups claim that the structural and metallic like defects are responsible for the Fermi level pinning using experimental techniques of scanning tunnelling microscopy (STM), inductively coupled plasma mass spectrometry (ICPMS) and X-ray photoelectron spectroscopy (XPS).[119,120] Direct measurement of Schottky barrier heights using atomic force microscopy (AFM) points out the metal-like defects like Mo vacancies and antisite defects decrease the pinning factor from 0.3 to 0.1, indicating a stronger Fermi level pinning.[121] Detailed studies using Raman spectroscopy and AFM reveal that the metal deposition on TMDs can generate the local mechanical strain and inhomogeneous metal clusters that deteriorate the electron injection efficiency.[122,123]

Even though the origin of the Fermi level pinning in TMDs remains controversial in the academic community, two theories, MIGS and bond polarization, that are widely used to explain the Fermi level pining in bulk materials have also demonstrated their effectiveness in 2D world.

2.4.2.1 Metal Induced Gap States Theory

The MIGS theory was first proposed by Heine[124] in 1965, and later developed by Tersoff.[125] The basis of this theory is that the tail of the metal electron wave function decays exponentially into the semiconductor bandgap and generates high interface density of states known as the metal-induced gap states. These states are found to be mostly donor-like near the valence band resulting in positive charges, while mostly acceptor-like near the conduction band with negative charges. E_{CNL} is the energy level at which the interface states change from mostly donor-like to acceptor-like. Figure 2-16 illustrates the metal/semiconductor junction when the metal Fermi level $E_{F.metal}$ is initially above E_{CNL} at the metal/semiconductor contact interface. The charge transfer through emptying the acceptor-like states or filling the donor-like state would create a dipole with the negative charge on the semiconductor side, which pulls the metal Fermi level ($E_{F.metal}$) to minimize the dipole charge towards zero and effectively aligns the $E_{F.metal}$ towards E_{CNL}.

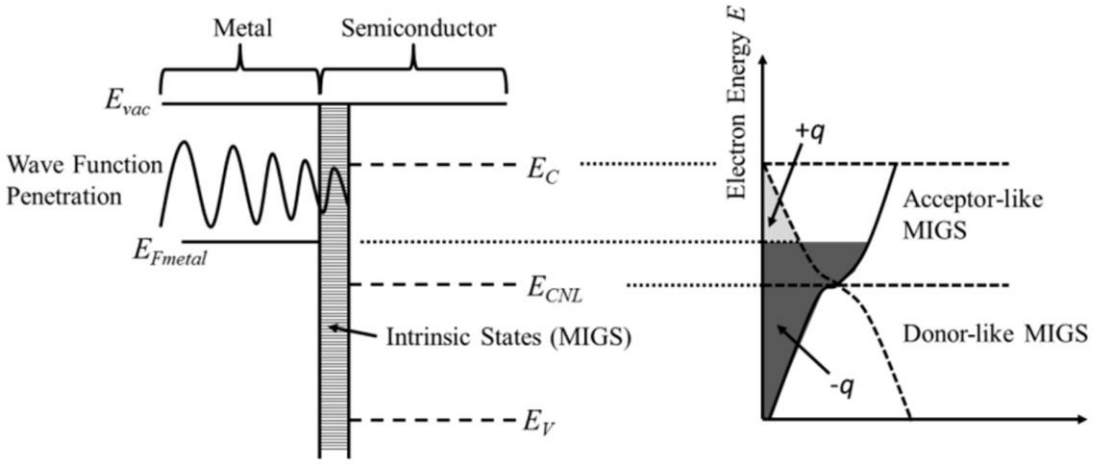

Figure 2-16 Fermi level pinning at the metal/semiconductor interface. The left side is the energy band diagram illustrating the generation of metal induced gap states. The right side shows the charging of the interface depending on the alignment of $E_{F.metal}$ and E_{CNL}. *Figure from Jacob et al.*[126]

The existence of the MIGS in 2D materials has been reported both experimentally and theoretically. Guo *et al.* provided a comprehensive DFT calculation of the Φ_{SB} of four TMDs with twelve metals covering a wide range of work functions, and the calculated Φ_{SB} follows the standard MIGS model despite van der Waals interlayer bonding.[111] This DFT simulation reveals that the top contact metal atoms are strongly bonded to the chalcogen atoms in TMDs, which is not van der Waals bonding as expected, while the formation of top contact bonds does not disrupt the interlayer M-X bonds of MoS_2 or WS_2 layer. A strong Fermi level pinning exists, and the pinning level is near the conduction band for MoS_2 and nearer mid-gap for other 2D TMDs. The pinning factor S is 0.3 for MoS_2 and is lower for other 2D materials. Recently, a study of ultrahigh vacuum STM (UHV-STM) to measure the atomic-scale energy band diagram of junctions between various metals and heavily doped MoS_2 further confirms the MIGS exists in 2D materials and dominantly accounts for the electronic properties of metal and TMDs junctions.[127] The MIGS decay lengths for three metal-MoS_2 junctions (Au, Pd, and graphite) were measured, and the decay lengths showed no dependence on the contact metal and were solely determined by the parameters of the semiconductor. This is the first experimental observation of the MIGS in 2D materials. Therefore, the Fermi level pinning is at least partially dependent on metal-

semiconductor interactions and the Schottky barrier height of TMDs largely follows the MIGS model like bulk semiconductors.

2.4.2.2 Dipole Formation Theory

In Tung's dipole formation theory,[128] when a semiconductor comes into contact with a metal, the wave functions of the two sides interact and form new wavefunctions at the interface where the electronic states are neither fully metal-like nor semiconductor-like, but rather a mixture of the two. The transition region between the metal and the semiconductor is called an interface specific region (ISR), as illustrated in Figure 2-17. The width of the ISR depends on the screening length, which is normally a few lattice spacings. In isolated bulk crystals, μ_M represents the internal chemical potential of the metal, and μ_M represents the internal ionization energy of the semiconductor, and the energetic positions of the bulk bands are completely determined once the crystal potential is known. The difference between the averaged electric potential cross the interface is the interface dipole ($e\Delta_{ISR}$). The Schottky barrier height is calculated through:

$$\Phi_{SB,p} = E_F^{\text{int}} - E_{VBM}^{\text{int}} = \mu_M - \mu_S - e\Delta_{ISR} \tag{2-10}$$

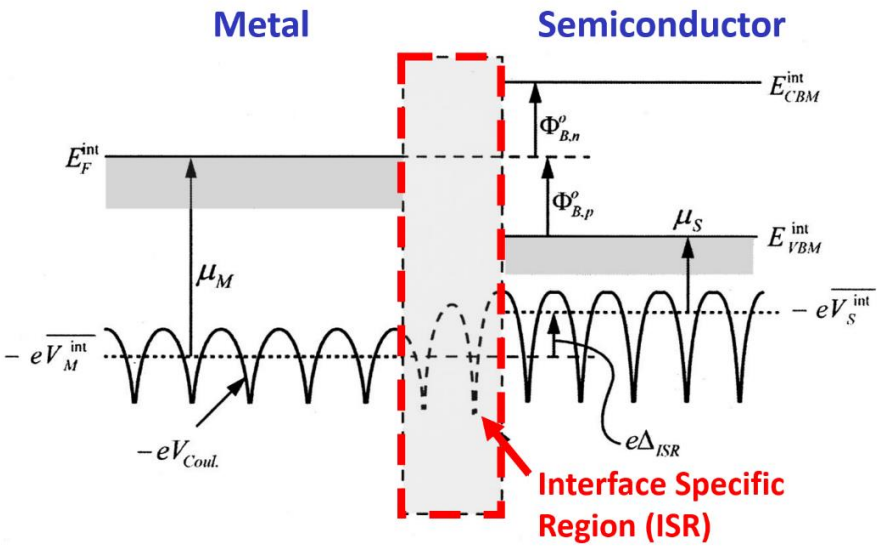

Figure 2-17 Energy band diagram and crystal potential distribution at a metal and semiconductor interface, illustrating the concept of the interface specific region. ***Figure from Tung et al.***[128]

When it comes to 2D semiconductors, the interface dipole formation exists as well. A study of metal/MoS_2 contacts by DFT calculations investigated a variety of metals with the work functions spanning over 4.2 ~ 6.1 eV and their contacts to MoS_2.[129] Based

on their calculations, the Fermi level pinning is caused by two following reasons: one is a metal work function modification by the adsorption of MoS_2 through an interface dipole because of interface charge redistribution; the other is the interface metal-S bonding weakens the intralayer Mo-S bonding because the metal contacts disturb the electron distribution surrounding S atoms, spilling band edge states into the gap states. As these states are dependent of metal, which is distinctly different from MIGS. It was found that the Fermi levels in all the studied metal-MoS_2 junctions are situated above the mid-gap of MoS_2 and the large deviation of the band alignment from the conventional Schottky-Mott model suggests significant band realignment due to the interface dipole formation.

2.4.2.3 Comparison of Theories

Both theories can explain the origin of Fermi level pinning and the change of Φ_{SB} after using some depinning methods (will be described later). The most significant difference between the MIGS Fermi level depinning and dipole induced barrier shift is the dependence of Φ_{SB} on the metal work function.[130] For MIGS theory, the high interface gap states are induced by the metal electron wave function when it decays exponentially into the semiconductor bandgap. If Φ_{SB} is found to reduce by different amounts depending on the metal work function, then the blocking of MIGS would be the underlying mechanism. As long as the inserted material is thick enough, the lowest achievable Φ_{SB} should only have a dependence on the metal. On the other hand, if the shift of Φ_{SB} has less dependence on the metal work function and the Φ_{SB} can either increase or decrease by depinning methods, then results would be ascribed to an interface dipole due to interface charge redistribution. Because the dipoles generated at the metal and semiconductor interface as well as the possible native oxide and dielectric interface might have different directions and magnitudes, which would bring more varieties to the modulation of Φ_{SB}.

2.4.3 Strategies to Lower Contact Resistances

As discussed above, the large contact resistance is the main factor that limits the performance of TMD devices and the further scaling down. A variety of strategies to alleviate the Fermi level pinning and lower the contact resistances have been reviewed here, including the use of metal or graphene as contacts, the insertion of dielectrics, edge contact geometry, and doping techniques.

2.4.3.1 Metal

According to previous discussion, the reduction of the Schottky barrier height can ideally be achieved *via* the selection of appropriate metals that ensure the easiest way of electron or hole injection. However, due to the Fermi level pinning effect widely observed in TMDs, the surface states pin the Fermi level into a certain level within a small range that makes the simple change of metal work functions ineffective to reduce the Schottky barrier height.

Regarding this situation, many studies on the choice of metals as well as the metal deposition method have been reported. Ultra-low work function metal like scandium contact (Φ_M =3.5 eV) has been proved to achieve the lowest contact resistances and highest electron injection among Sc Ti, Ni, and Pt.[112] By contrast, ultra-high work function metal like MoO_x (x<3, Φ_M =6.6 eV) facilitates effective hole injection, and large improvement of on-current has been observed in p-type MoS_2 FETs over devices of Pd contacts even though the contact resistance is relatively high (200 kΩ·μm).[131] However, note to mention that the pinning factor extracted from their experimental results is 0.1 for MoS_2, indicating little effect that the metals could have on the Schottky barrier height and the presence of the strong Fermi level pinning effect. From DFT calculations, the adsorption of MoS_2 on the metal surfaces and the metal-S interaction during the metal deposition process are possible origin of the Fermi level pinning.[129] There are two methods to eliminate the Fermi level pinning. One method is to strengthen the hybridization and further metallization of TMDs underneath the metal contacts. It was also found that metals with strong hybridization with TMDs can form good contacts of low contact resistances. A study on WSe_2 FETs using Ti, In, and Ag contacts reveals that Ag contact to multilayer WSe_2 has the lowest contact resistance due to the d-orbital overlap in metal Ag and WSe_2 indicating the diffusion of Ag into MoS_2 and doping the WSe_2.[132] Significant reduction of Schottky barrier height and improvement of the contact resistances have also been observed in monolayer MoS_2 FETs with molybdenum contacts owing to the strong covalent bonding between metal Mo and MoS_2 semiconductor, with a reduction in the contact resistance down to 2 kΩ·μm.[133] The other method is to weaken the hybridization by inserting graphene or dielectrics which will be discussed in the later sections, or form van der Waals-contacted MoS_2 FETs by a metal transfer method to minimize the interface disorder and metal-semiconductor interaction caused in the conventional metal evaporation process (Figure 2-18).[134] This study offers a completely new idea of fabricating the S/D contacts

for FETs, and the metal-semiconductor junction without any chemical bonding shows great advantages in depinning the Fermi level, approaching the Schottky-Mott limit (S=0.96) and realising the fully tunable Schottky barrier height by the metal work functions.

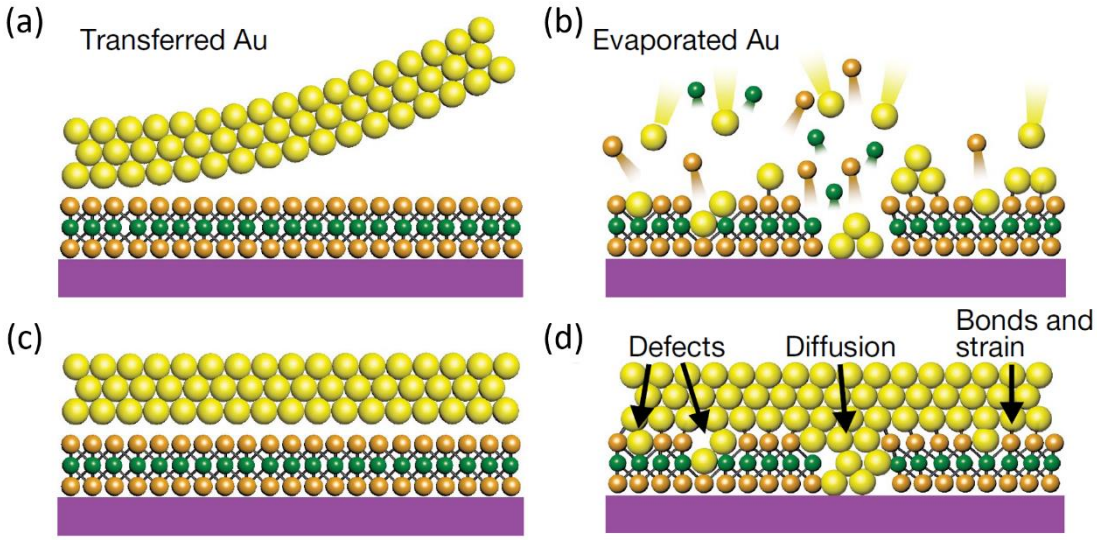

Figure 2-18 Cross-sectional schematics of the comparison between (a&c) metal transfer method and (b&d) traditional metal evaporation method. ***Figure from Liu et al.*** **[134]**

2.4.3.2 Graphene

As a transparent semi-metal, graphene demonstrates its exciting potential in Schottky-junction based applications when contacting conventional semiconductors like Si.[135] Considerable efforts have been devoted to apply graphene as an interfacial layer to form a contact to 2D semiconductors. The two main advantages of graphene contacts involve (1) the interaction of graphene and TMDs is combined with van der Waals forces free from gap states and surface modification; (2) the Fermi level of graphene can shift up and down with the applied gate voltage thus facilitating either electron or hole injection.[136]

Inspired by the silicon/graphene barristor[135] and the h-BN/graphene/h-BN heterostructure,[137] the first integration of graphene and TMDs is a vertical FET based on graphene/WS_2 heterostructures,[138] followed by all 2D transparent lateral MoS_2 FETs (Figure 2-19)[139] and WSe_2 thin film transistors (TFTs)[140] built from h-BN as the top-gated dielectric, and graphene as the S/D electrodes and the top-gated contacts, or using ionic liquid gating to improve the graphene tunability.[141] At the same time, a systematic comparison of the graphene/MoS_2 heterojunction contact to the conventional

metal/MoS_2 junction has been conducted on the first large-scale platform for 2D electronics.[142] The contact resistance ranges from 3.7 ~ 100 kΩ·μm due to the inevitable solvent and organic residues from PMMA.[139,142,143] Later, dry transfer method has been adopted using polymer layers like PMMA/polymer cement concrete (PCC) stack or poly(dimethylsiloxane) (PDMS), and the contact resistance can be reduced down to 0.2 ~ 2 kΩ·μm.[144,145] Furthermore, the work function of graphene can be modulated by electric field based on the equations: [146]

$$W_{M-g} = E_F = -\mathrm{sgn}(n_0)\hbar v_F \sqrt{\pi |n_0|} \qquad n_0 = q(V_{GS} - V_{TH}) \tag{2-11}$$

where n_0 is the carrier concentration in graphene, $\hbar$ is Planck's constant, and v_F is the Fermi velocity. They found a change of 30 V in the gate voltage can result in 200 mV change in the graphene work function (300 nm SiO_2 as the gate dielectric). Owing to the tunability of the graphene work function by the applied gate voltage, barrier free even negative barrier have been achieved in graphene/MoS_2 heterostructured FETs.[147,148] Further applications of graphene/TMD heterojunctions have been reported on inverters and negative-AND (NAND) gates in high-speed logic circuits[149] and photodetectors.[150]

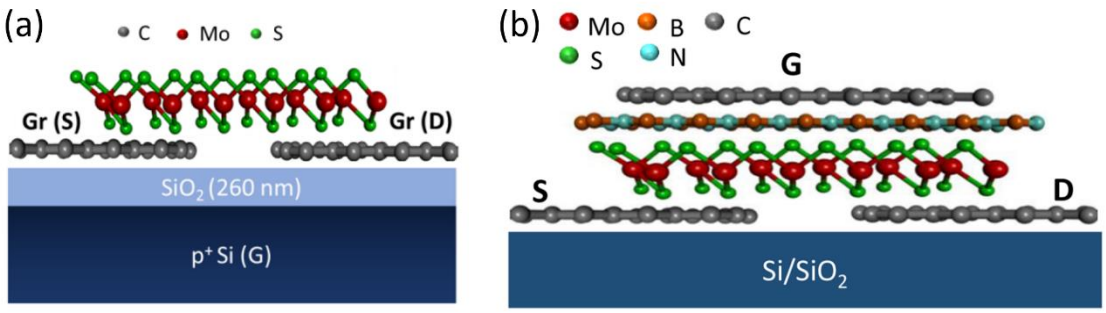

Figure 2-19 (a) Back-gated few-layer MoS_2 FET with monolayer graphene contacts. (b) All-2D MoS_2 FET with few-layer h-BN gate dielectric, bilayer graphene S/D contacts and multilayer graphene as top-gated electrodes. *Figure from Roy et al.*[139]

2.4.3.3 Dielectric

One novel method to alleviate the Fermi level pinning in bulk semiconductors is to insert an ultrathin dielectric layer between metal and semiconductor. This metal-insulator-semiconductor (MIS) sandwich structure can effectively block the exponential electron wave function decay in the semiconductor thus reducing the MIGS density. The additional dipoles formed at the interface can also attenuate the charge penetration and reduce the bending of the band structure.

This MIS contact structure was first introduced to monolayer MoS_2 FETs with a thin MgO interfacial layer between the Co electrodes and MoS_2 flakes. It demonstrates that the Schottky barrier height can be manipulated by both the dielectric thickness and back-gate voltage, and the reduction in the Schottky barrier height can be as much as 84%.[151] Following the first study, other insertion layers such as TiO_2[113,152–156] or Al_2O_3[152,157] were also found effective in reducing the contact resistance in MoS_2 FETs. A recent study analysed the depinning effect of TiO_2 interfacial layers on MoS_2 FETs with four metals, they found this MIS contact can widen the controllable Schottky barrier height ranges from 37 meV to 344 meV thus depinning the Fermi level.[155] The Fermi level depinning has also been observed in WS_2 FETs when inserting an ultrathin TiO_2 layer (Figure 2-20), as a result, a low work function metal like Ti would result in electron injection while a high work function metal like Pd would facilitate hole injection.[116] Note that these studies are only using a dielectric interfacial layer of a certain thickness, and a comprehensive and statistical study of the influence of the dielectric thickness (Ta_2O_5 in their case) on the Schottky barrier height has been further reported.[158] This work reveals that there exists an optimal thickness in the inserted dielectric as the modulation of the contact resistance *via* a dielectric is a trade-off between the resistance due to the Schottky barrier height and the resistance due to tunnelling through the dielectric. By varying the thickness of Ta_2O_5 from 0 to 5 nm, they found the lowest Schottky barrier height (29 meV) and contact resistance were achieved at 1.5 nm Ta_2O_5. Besides these bulk dielectrics, recent studies have demonstrated that 2D dielectric h-BN works as an effective interfacial layer to reduce the Schottky barrier height. A reduction of the Schottky barrier height from 158 meV to 31 meV has been observed for Ni contacts to MoS_2 with 1 ~ 2 layer of CVD grown h-BN.[159] Nearly barrier free (16 meV) Ohmic contacts at low temperature have been achieved using Co/h-BN/MoS_2 MIS contacts.[160] This is because the insertion of monolayer h-BN can break the interaction between the metal and MoS_2 thus eliminating the interface states that cause the Fermi level pinning as a DFT calculation indicates.[161] Additionally, the inserted h-BN layer can decrease the metal work function by 2 eV for large work function metals like Co and Ni due to lattice matching with h-BN,[161] which has been confirmed in their XPS measurements.

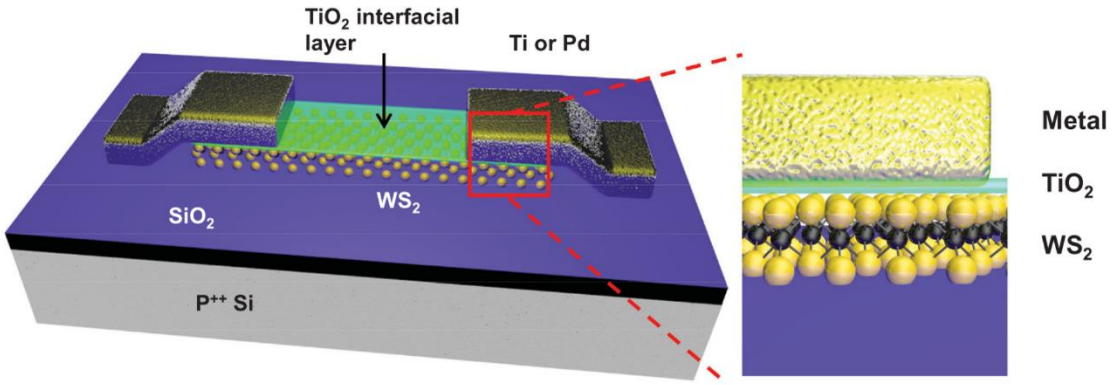

Figure 2-20 Schematic of a back-gated WS_2 FET with a TiO_2 interfacial layer inserted between the metal and WS_2 at S/D contacts. ***Figure from Park et al.*****[116]**

2.4.3.4 Edge Contact

Besides the top contact geometry, edge contacts can be another exciting choice. DFT calculations have modelled these two contact geometries, and found the edge contact can offer more efficient carrier injection and smaller contact resistances to atomically thin TMDs owing to a smaller contact area defined by their atomic thickness.[118] In the top contact geometry, the carrier injected from metal electrodes flows through a wide tunnel barrier in the layers *via* undesirable out-of-plane carrier transport, while the edge contact geometry enables in-plane carrier injection with smaller tunnel barrier widths.[8]

The one-dimensional (1D) edge contact was first fabricated in a h-BN/graphene/h-BN structure and the capping layer h-BN could protect the top of the channel from forming direct top contacts to the deposited metals. A low contact resistance down to 0.1 kΩ·μm was achieved at room temperature using this method.[137]

Although the edge contact geometry demonstrates its capacity to obtain smaller contact resistance than that of top contacts, the fabrication process to realize the pure edge contact is very difficult and complicated. Therefore, few works have been reported on the edge contacts to TMDs. One application of this h-BN encapsulated graphene edge contact has been realized in MoS_2 multi-terminal devices as schematically shown in Figure 2-21.[145] A low contact resistance of 2 kΩ·μm can be achieved at high applied voltage at room temperature, and can be further reduced to 0.7 kΩ·μm at low temperature. Another study explored the possibility of fabricating the edge contact of metals on MoS_2 encapsulated under Al_2O_3 thin film.[162] Given the difficulties in the fabrication of edge contacts, laterally stitched graphene/TMD, h-BN/TMD, and

TMD/TMD heterostructures have been synthesized in scalable and patternable CVD growth.[149,163]

However, the contact resistance of 1D graphene contact to MoS_2 ranges from 30 ~ 300 kΩ·μm, which is several orders of magnitude higher than the state-of-art contact resistance values. So, the edge contact faces many challenges now and enormous efforts are still needed to simplify the fabrication process and optimize the direct synthesis of 2D heterostructures.

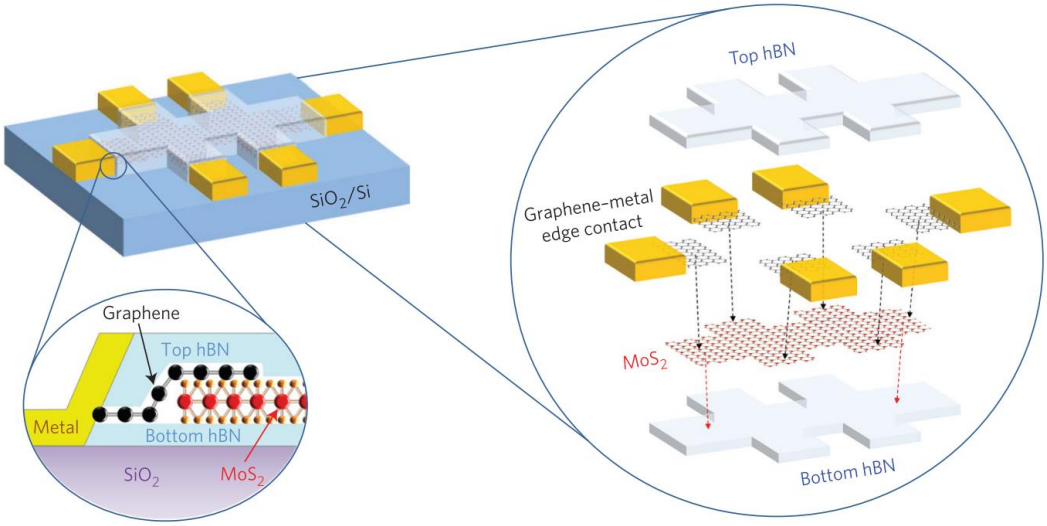

Figure 2-21 Schematic of h-BN encapsulated MoS_2 multi-terminal devices with one-dimensional edge contacts to graphene. *Figures from Cui et al.*[145]

2.4.3.5 Doping Technique

Doping technique is a traditional method to reduce the Schottky barrier height in bulk semiconductors. By heavily doping the semiconductor underneath metals, electrons can easily tunnel through the barrier.[164] Due to the atomically thin thickness of TMDs, the conventional method of ion-implantation becomes challenging to control, instead, surface modification *via* molecules or ions is a more popular method to dope 2D materials.

Several studies have demonstrated that heavily doping TMDs can reduce the contact resistance. Molecules or ions have been used to dope TMDs including PEI,[165] benzyl viologen molecular doping,[166] chloride molecular[167] and lithium fluoride.[168] A typical doping process is to soak the TMD flakes in a certain solution for several hours as shown in Figure 2-22a. Electron would transfer from the donor (BV) to the acceptor (MoS_2) due to the energy level offset (Figure 2-22b). The contact resistance ranges from 0.5 ~ 1.1 kΩ·μm when doping with the above-mentioned molecules and ions. Besides

the solvent doping, gas driven doping has been studied including O_2 and N_2 gas environment under deep ultraviolet light[169] and high-pressure H_2 annealing.[170] In spite of the enhanced carrier density and mobility compared to the non-treated samples, the contact resistance is 14.6 kΩ·μm, which is higher than those obtained from the solvent doping. Unfortunately, the air instability of chemical doping is still a serious problem to form highly reliable contacts, because the easy detachment of the absorbed chemical species may happen and the reaction with oxygen and water could not be avoided when devices being exposed in the ambient air for a long time.[171]

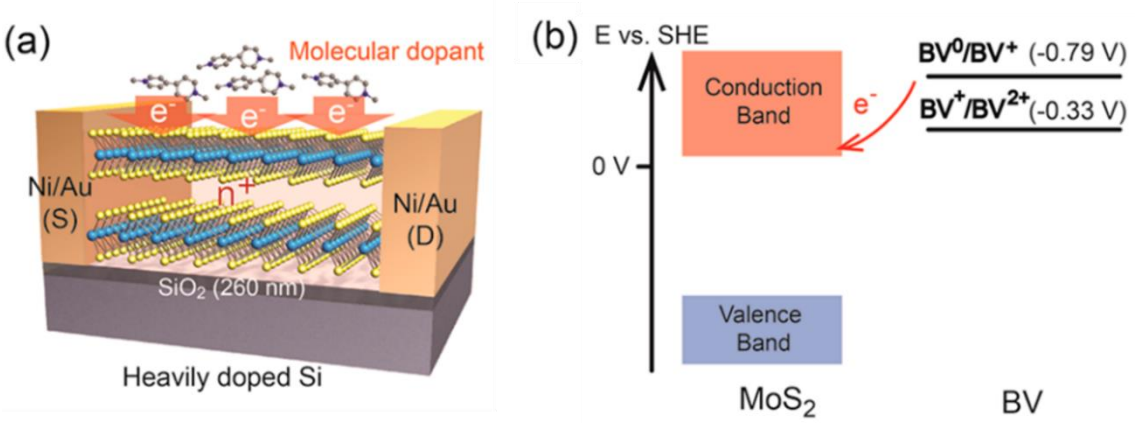

Figure 2-22 (a) Schematic illustration of a back-gated MoS_2 device used for benzyl viologen (BV) surface charge transfer doping studies. (b) Energy band diagram of MoS_2 and BV redox states. Electron donation occurs from BV molecules to MoS_2 due to the energy level offset. ***Figure from Kiriya et al.*[166]**

2.4.4 Extraction of Schottky Barrier Heights

2.4.4.1 Flat Band Condition

The accurate Schottky barrier height Φ_{SB} is extracted at the flat band condition (V_{GS}=V_{FB}). Note that the Φ_{SB} of this work cannot be treated the same as the Φ_{SB} of the conventional metal/semiconductor contact, in which the insulator is not taken into consideration in the thermionic emission equation for the current-voltage characteristics of a metal/semiconductor junction. Therefore, the Φ_{SB} extracted in this work reflects the overall electrical transport behaviour. Figure 2-23 illustrates the reason why the flat band condition can be used to extract an accurate Φ_{SB} based on a MOS diode and thermionic emission theory. When a metal, a semiconductor and an oxide are in an isolated situation, all bands are flat as shown in Figure 2-23a, and this is called the flat band condition. However, for commonly used metal electrodes, the work function

difference of the metal and the semiconductor is generally not zero, so charges inside the oxide or at the oxide-semiconductor surface will lead to the band bending. In thermal equilibrium, two basic requirements in the construction of the energy band diagram are (1) the Fermi level must be a constant on both sides of the interface, and (2) the vacuum level must be continuous and parallel to the band edges. To accommodate the work function difference, the semiconductor bands bend downward as shown in Figure 2-23b. So, the metal side is positively charged and the semiconductor side is negatively charged. To obtain an ideal flat band condition shown in Figure 2-23c, a negative voltage V_{FB} must be applied to the metal, and this voltage is called the flat band voltage, which is given by

$$V_{FB} = \left(\Phi_M - \Phi_S\right)/q = \left(\Phi_M - \chi - E_C + E_F\right)/q \qquad (2\text{-}12)$$

At the flat band condition, (1) the energy difference between the metal work function Φ_M and the semiconductor work function Φ_S is zero, (2) the electric filed in the oxide is zero, and there is no carrier transport through the oxide. Therefore, the Φ_{SB} extracted at the flat band condition can reflect the accurate situation of metal/semiconductor contact by ruling out other factors such as any trap state density that can change the Φ_{SB} .

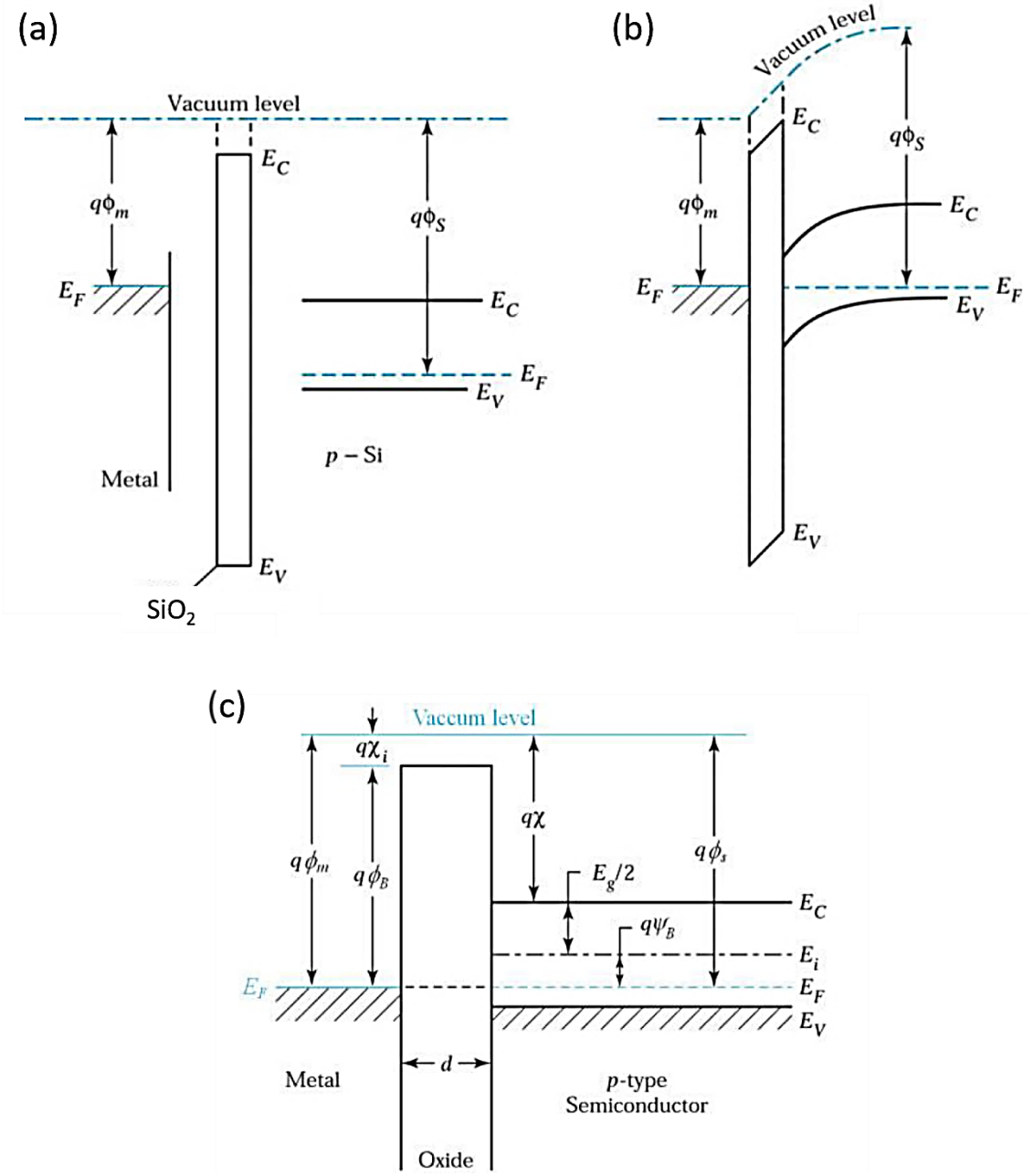

Figure 2-23 Energy band diagram of (a) an isolated metal and an isolated semiconductor with an oxide between them; (b) a MOS diode in thermal equilibrium; (c) a MOS diode at the flat band condition. *Figures from S. M. Sze et al.*[172]

For TMD FETs, the total current is a combination of the thermionic emission current and thermally assisted tunnelling current, and the composition of these two components depends on the applied gate voltage (V_{GS}).[112,158,173,174] Figure 2-24a shows a typical transfer characteristic of a FET with coloured circles referring to different transport regimes. Specifically, the thermionic region and the tunnelling region are separated by a transition turning point called the flat band voltage (V_{FB}). In the electron

thermionic region (V_{GS}<V_{FB}), a pure thermionic emission current makes up the whole current and the barrier to flow through is defined by the conduction band in the semiconductor channel (Figure 2-24b). By applying a more negative V_{GS}, the conduction band is higher thus the increased barrier resulting in the exponential decrease of the current. The effective thermal injection barrier is the sum of the accurate Schottky barrier height (Φ_{SB0}) and the surface potential ($q\psi_s$). As discussed earlier, $q\psi_s$ would be zero at the flat band voltage (Figure 2-24c), thus the extracted Schottky barrier height at this point would be the accurate one. In the electron thermally assisted tunnelling region (V_{GS}>V_{FB}), the current consists of thermionic emission current and thermally assisted tunnelling current in Figure 2-24d,e. When the flat band voltage is reached, the thermionic component of electron current no longer increases exponentially with the increase of V_{GS} as indicted by the red dash line in Figure 2-24a because the barrier for thermionic emission of electron is fixed at Φ_{SB0}. On the other hand, the further increased V_{GS} induces the downward bending of the bands, thus the tunnelling barrier becomes thinner and even almost transparent beyond the threshold voltage (V_{GS}>V_{TH}) as shown in Figure 2-24e.

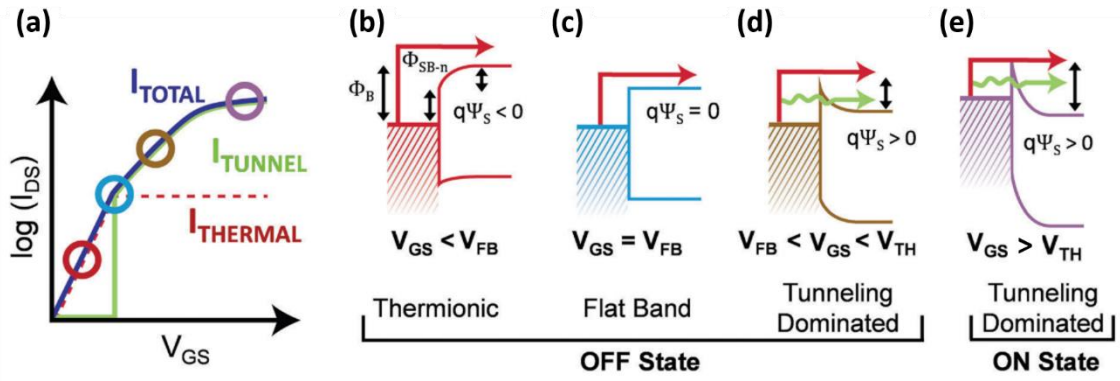

Figure 2-24 (a) Transfer characteristic of a typical FET. The coloured circles are four regimes including the thermionic region (red), flat band condition (blue), OFF state tunnelling dominated region (brown), and ON state tunnelling dominated region (purple). (b-e) The corresponding band diagrams for the four regimes. *Figure from Schulman et al.*[8]

Therefore, the extracted overall barrier heights in the tunnelling region above the V_{TH} would be considerably low because of the tunnelling carrier injection added into the total current. Moreover, this also illustrates the importance of choosing the right gate

bias to extract the Φ_{SB}, because in the region above the threshold voltage, the extracted value can easily result in a very small value due to the additional tunnelling current, however this tunnelling component is not included in the standard thermionic emission theory.

2.4.4.2 Extraction Methods

The above band diagram analysis can demonstrate that the tunnelling current can only be ignored when the applied gate voltage is below the flat band voltage, and the accurate Schottky barrier height Φ_{SB0} can be obtained once the V_{FB} is identified. In a FET geometry, the S/D electrodes are two Schottky diodes connected back-to-back and most of the voltage drop is consumed at the reverse-biased contact (source side of an n-type FET) that dominates the transistor behaviour. The current injected through a reverse-biased Schottky barrier obeys the thermionic emission equation:[175,176]

$$I_{DS} = AA^{*}T^{2}\exp\left(-\frac{q\Phi_{SB}}{k_{B}T}\right)\left(\exp\left(\frac{qV_{DS}}{k_{B}T}\right)-1\right) \tag{2-13}$$

where I_{DS} is the drain-source current, A is the contact area, A^{*} is the Richardson's constant, T is the temperature, k_B is the Boltzmann constant, q is the electronic charge, Φ_{SB} is the effective Schottky barrier height, and V_{DS} is the drain-source voltage.

One method to extract Φ_{SB} is to plot an Arrhenius plot when $V_{DS} >> k_{B}T/q$, which can be written by:[175,177]

$$\ln\left(\frac{I_{DS}}{T^{2}}\right) = \ln(AA^{*}) - \frac{q\left(\Phi_{SB}-V_{DS}\right)}{k_{B}}\frac{1}{T} \tag{2-14}$$

A plot of $\ln\left(I_{DS}/T^{2}\right)$ *versus* $1/T$ at a constant drain bias voltage has a slope of $-q\left(\Phi_{SB}-V_{DS}\right)/k_B$ and an intercept $\ln(AA^{*})$ on the vertical axis. Φ_{SB} can be extracted from the linear fit slope and can avoid the uncertainty of A^{*}. However, this varied-temperature method also faces its own problem, that is the three basic assumptions which validate the use of the Arrhenius plot involve (1) $V_{DS} >> k_{B}T/q$; (2) contact resistance dominates the overall resistance, and (3) thermally assisted tunnelling current is negligible.[6] The verification of these assumptions is neglected in many papers. For example, V_{DS} is close to $k_{B}T/q$ (~ 25.2 mV at room temperature) and a high tunnelling current leads to the underestimation of the Φ_{SB} using the Arrhenius plot.

Based on Equation (2-13), Φ_{SB} can also be extracted from the following expression using a fixed-temperature method:[177]

$$\Phi_{SB} = \frac{k_B T}{q} \ln\left(\frac{AA^* T^2 \left(\exp\left(\frac{qV_{DS}}{k_B T} \right) - 1 \right)}{I_{DS}} \right) \tag{2-15}$$

Note that the most uncertain parameter in Equation (2-15) is A^*, whose accuracy determines the extracted Φ_{SB}. A^* is often calculated using a theoretical value by $A^* = 4\pi q m^* k_B^2 / h^3 = 120(m^*/m)$,[175] where m is the free electron mass and m^* is the effective electron mass. Because A^* is in the natural logarithm term, even if the value of A^* increased or decreased by a factor of 10, the error in the value of Φ_{SB} will be about ±60 meV at room temperature. The calculation can be expressed by $\Delta\Phi_{SB} = \Delta\Phi_{SB1} - \Delta\Phi_{SB2} = k_B T / q \ln(A_1^* / A_2^*)$. Therefore, the variation in A^* does not have considerable effect on the value of Φ_{SB} and this fixed-temperature method can offer a close estimation to Φ_{SB}. To suppress the underestimation effect from the tunnelling current, the device needs to work at the flat band condition. A more reliable and accurate method is to plot the extracted Φ_{SB} *versus* gate bias.[112]

Consider the sub-threshold region, where the gate bias is below the threshold voltage, and the semiconductor is in weak inversion of depletion. A quadratic equation describes the Φ_{SB} in the sub-threshold region can be given as:[178]

$$V_{GS} - V_{FB} = \Phi_{SB} + \frac{\sqrt{2\varepsilon_s q \Phi_{SB} N_A}}{C_{ox}} \tag{2-16}$$

where ε_s is permittivity of semiconductor, N_A is acceptor impurity concentration, and C_{ox} is the oxide capacitance. From Equation (2-16), the relative change of V_{GS} and Φ_{SB} is calculated to be:

$$\frac{dV_{GS}}{d\Phi_{SB}} = 1 + \frac{1}{C_{ox}} \sqrt{\frac{\varepsilon_s q N_A}{2\Phi_{SB}}} = \frac{C_{ox} + C_D + C_{it}}{C_{ox}} \tag{2-17}$$

The definition for the sub-threshold swing (S) is the gate-voltage change needed to induce a drain-current of one order of magnitude, and it can tell how sharply the transistor is turned off by the gate voltage. By definition, the sub-threshold swing can be calculated as:[178]

$$
\begin{aligned}
S &\equiv (\ln 10)\frac{dV_{GS}}{d(\ln I_{DS})} = (\ln 10)\frac{dV_{GS}}{d(\beta\Phi_{SB})} \\
&= (\ln 10)\frac{k_B T}{q}\left(\frac{C_{ox}+C_D+C_{it}}{C_{ox}}\right) \\
&= (\ln 10)\frac{k_B T}{q} n \qquad n = 1+\frac{C_D+C_{it}}{C_{ox}}
\end{aligned}
\tag{2-18}
$$

Equation (2-17) can be written as:

$$
\frac{d\Phi_{SB}}{dV_{GS}} = \frac{C_{ox}}{C_{ox}+C_D+C_{it}} = \frac{1}{n} \tag{2-19}
$$

Integrating Equation (2-19), the effective Schottky barrier height (Φ_{SB}) can be expressed as:[112,178]

$$
\begin{aligned}
\Phi_{SB} &= \Phi_{SB0} - (V_{GS} - V_{FB})/n \qquad for \quad V_{GS} \le V_{FB} \\
\Phi_{SB} &= \Phi_{SB0} - \Delta \qquad\qquad\qquad for \quad V_{GS} > V_{FB}
\end{aligned}
\tag{2-20}
$$

where Φ_{SB} is the effective Schottky barrier height, Φ_{SB0} is the accurate Schottky barrier height. *n* represents the fraction of the applied gate voltage that contributes to the interface potential, C_{ox} is the oxide capacitance, C_D is the channel depletion layer capacitance, C_{it} is the interface trap capacitance. Δ is a positive (not constant) quantity that describes the situation for $V_{GS}>V_{FB}$, the extracted barrier height is smaller than Φ_{SB0} due to additional thermally assisted tunnelling current through the device. Equation (2-20) shows a linear relation is expected between Φ_{SB} and V_{GS} for $V_{GS}\le V_{FB}$, and the Φ_{SB} extracted at the flat band voltage is at point of inflection of the linear line.

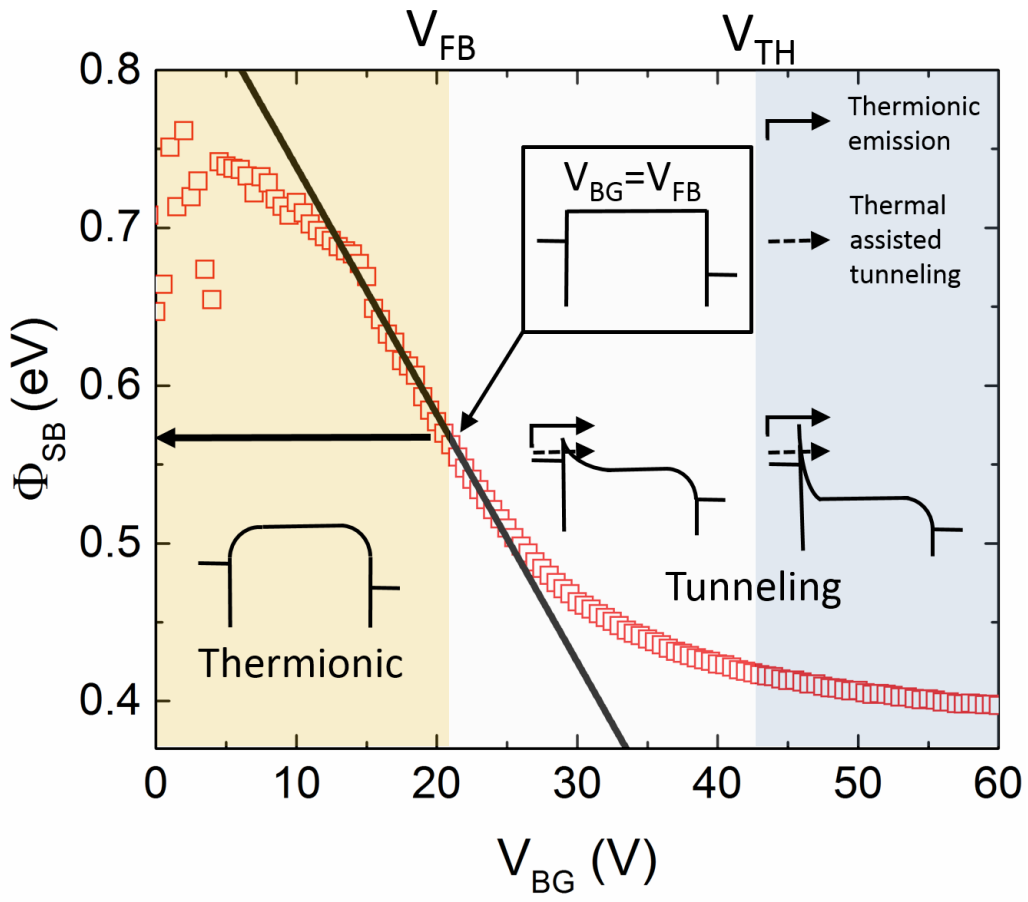

Figure 2-25 Example of extracting the accurate Schottky barrier height (Φ_{SB0}) of a back-gated WS_2 FET with Pd contacts at drain-source voltage (V_{DS}) of 100 mV. The insets show the band diagrams when the back-gate bias (V_{BG}) varies in three regions: below flat band (V_{FB}, yellow area), below threshold (V_{TH}, white area), and above threshold (blue area).

Figure 2-25 shows an example of this extraction method using the transfer characteristic of the back-gated WS_2 FET with Pd contacts. Φ_{SB} was extracted using the fixed-temperature method at various gate biases to obtain a plot of Φ_{SB} *versus* gate bias. By drawing a linear plot as shown in Figure 2-25, the flat band condition V_{FB} can be identified where the plot deviates from the linear relationship, and the accurate Schottky barrier height Φ_{SB0} is the Φ_{SB} at V_{FB}. This extraction method has been used in the following research.

3 EXPERIMENTAL DETAILS OF SYNTHESIS, FABRICATION, AND CHARACTERIZATION

This chapter presents the main experimental methods used in this research, including the microwave PECVD system for graphene synthesis, the ALD system for dielectric deposition, the transfer procedures of 2D materials, the device fabrication procedures, and the characterization techniques.

3.1 Microwave PECVD System

Chemical vapour deposition (CVD) is the deposition of a solid material on a heated surface from a chemical reaction in the vapour phase. Based on the different supply of energy sources in the CVD process, CVD can be classified in three categories: thermal CVD, laser-assisted CVD, and plasma-enhanced CVD, using heat, light, and electric discharge, respectively.

Low-temperature synthesis of high-quality graphene is a great challenge facing the academic research and industrial production. Unlike thermal CVD relying on the thermal energy, the reaction in PECVD is activated by plasma. Plasma is one of the four fundamental states of matter and can be created by heating a gas or subjecting it to a strong electromagnetic field. It is a collection of freely moving charged particles, including ions (positive charged), electron (negative charged), and atoms that have not been ionized (neutral), which is electrically neutral on the average.[179] These high-energy

particles collide with the gas molecules, resulting in dissociation and generation of reactive chemical species and the initiation of the chemical reaction, which allow the deposition to happen at much lower temperature compared to thermal CVD. Therefore, PECVD plays a significant role in the development of graphene synthesis at low temperature. This enables graphene grown on the various surfaces such as the coating of low-temperature substrates (which might otherwise melt), organic polymers (which might otherwise degrade and outgas), and metals which experience structural changes at high temperature.[180] Moreover, the low-temperature growth can avoid the stresses caused by the thermal expansion mismatch between the substrate and the grown film in the high-temperature growth.[180] These two advantages make PECVD very suitable to synthesize graphene at lower temperature and improve the uniformity and quality of graphene at the same time.

Figure 3-1 shows a typical PECVD process for metal-catalyst free growth of graphene that involves the following steps:[45]

- Ramping step: heating the substrate in the vacuum up to the pre-process temperature.
- Annealing step: maintaining the temperature and introducing the hydrogen flow. Igniting the plasma and controlling the pressure and electric field until a stable plasma is obtained. The surface of the dielectrics can be modified and cleaned before the growth.
- Growing step: introducing new precursors as carbon sources to grow graphene over the substrates. Dissociation and activation of the precursors occur in the presence of the plasma. During the growth, many parameters need to be optimized such as the pressure, mixture ratio of gases, gas flow rate, growth time, and temperature.
- Cooling step: switching off the plasma and cooling the reactor in a proper atmosphere under 200°C to prevent graphene functionalization with oxygen-containing groups.
- Final step: backfilling with inert gases (N_2) up to atmospheric pressure and open the reactor chamber.

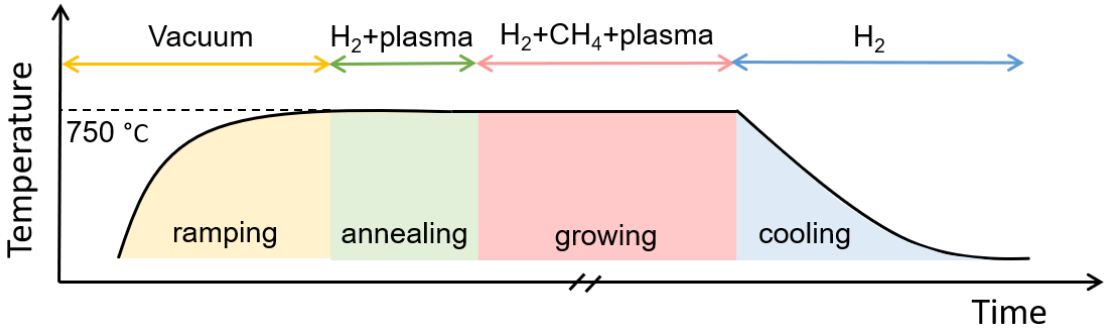

Figure 3-1 Schematic PECVD process for direct growth of graphene on insulators.

According to different power frequencies, plasma sources can be classified into microwave plasma (normally 2.45 GHz), radio frequency (RF) plasma (normally 13.56 MHz), and direct current (DC) plasma. The advantage of microwave PECVD over RF PECVD is that its etching effect is weaker. When the microwave frequency is used, plasma is produced by the application of a high frequency electric field of magnitude of 2.45 GHz at a low pressure to a carrier gas such as argon or nitrogen. At such a high-frequency electric field, the electrons, with extremely small masses, are quickly accelerated to high-energy level, while the heavier ions with much greater inertia cannot respond to the rapid changes in the electric field direction and remain in lower temperature and energy level. Compared to the microwave PECVD, the RF PECVD uses lower-frequency electric field (13.45 MHz), so the ions with lower energy can better respond to the relatively slowly changing field direction and become highly dissociative ions. The RF plasma is usually generated at higher pressure, and the mean free path is greatly reduced. So, the collisions are more frequent and too much atomic hydrogen might be produced, resulting in too strong etching effect for the graphene growth.

The PECVD system used in this research is a homemade microwave PECVD, which mainly consists of a microwave generator, power monitor, antenna, reaction chamber, gas lines, pumping system, heating system, and control panel. This is a transverse magnetic mode microwave reactor, where the dominant wave is in a cylindrical waveguide, as Figure 3-2 shows. An antenna is introduced at the top of the synthesis reactor vessel, a cylindrical cavity, through a coaxial port, to produce a more intense electric field on the central part of the substrate, where a plasma ball can be clearly observed.[181] The substrate of a transverse magnetic microwave reactor is below the plasma ball with a honeycomb mesh shield to protect the samples from the ion-

induced damage of the plasma ball, while the energetic and reactive species could pass through the mesh shield and reach the substrates to synthesize graphene.

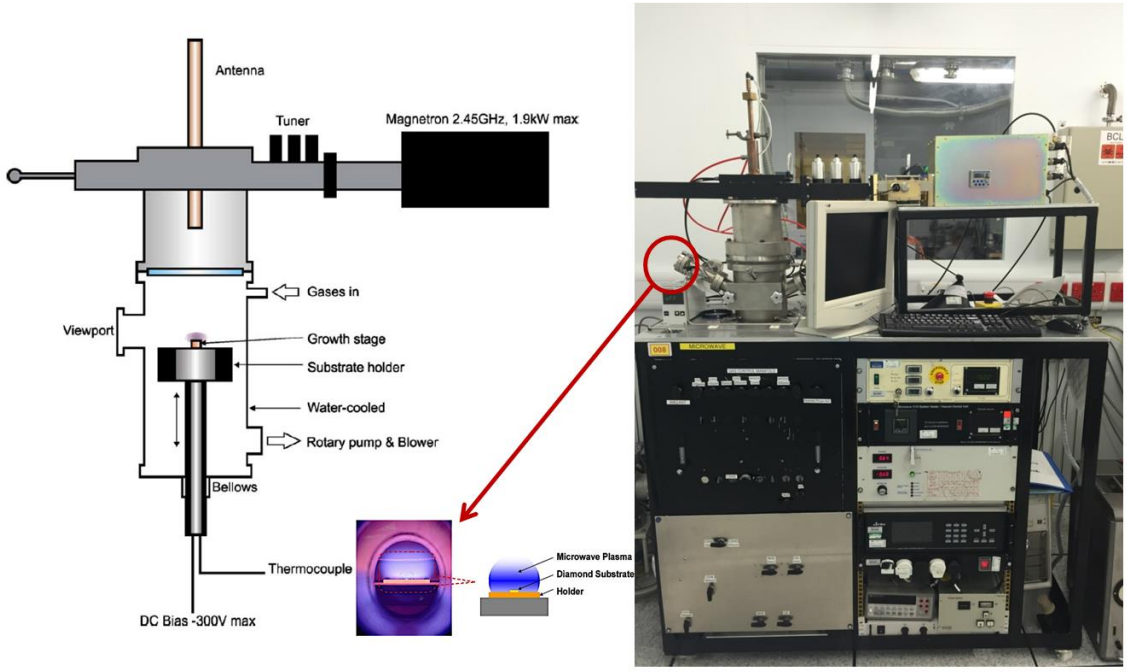

Figure 3-2 Left: schematic illustration of microwave PECVD system. Right: photo of the microwave PECVD in the CAPE cleanroom.

3.2 Atomic Layer Deposition System

Atomic layer deposition (ALD) is a self-limiting vapour-phase thin film deposition method. In contrast to CVD, ALD relies on saturating and irreversible, separated gas-solid reactions, which are repeated in a cyclic manner.[182] This unique deposition design makes ALD suitable for atomic layer control, good uniformity and conformal deposition using sequential, self-limiting surface reactions.[183]

A typical ALD process consists of four steps,[182] and this process is then cycled until the appropriate film thickness is achieved, as schematically illustrated in Figure 3-3.

- Step 1a: gas-solid reaction. A metal precursor (reactant A) is introduced in the vapour phase by an inert carrier gas into the reaction chamber, where it adsorbs to reactive surface sites upon the substrate.
- Step 1b: purge process. Once the surface sites have been fully occupied, the surface is saturated, and an inert gas purge is to remove the unreacted precursor and gaseous by-products.

- Step 2a: gas-solid reaction. A pulse of a second vapour non-metal precursor (reactant B) subsequently reacts with surface adsorbed by reactant A to produce the desired thin film.
- Step 2b: purge process. A second inert gas purge is then performed to remove additional unreacted precursor and by-products.

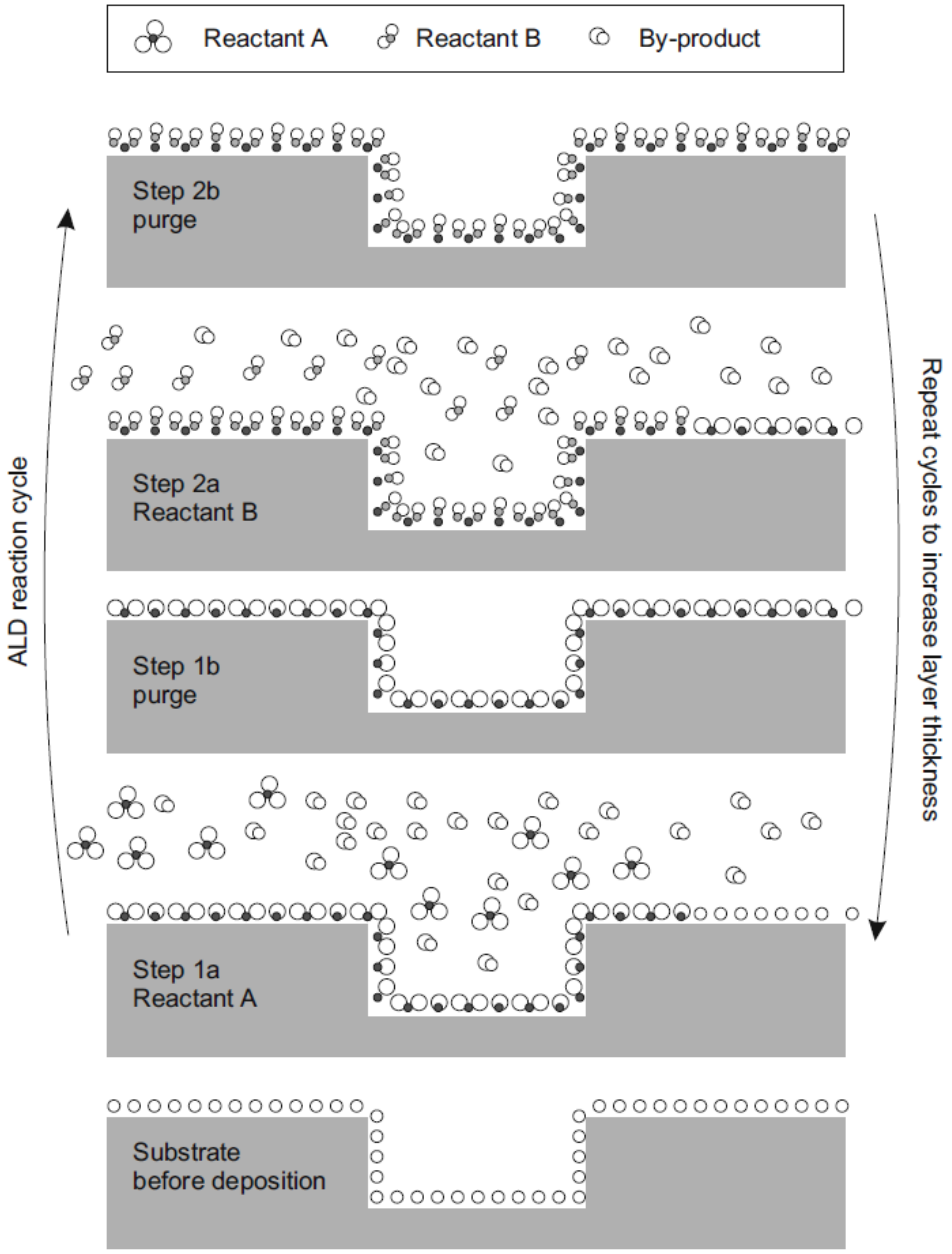

Figure 3-3 Schematic illustration of one ALD reaction cycle. Figure from Miikkulainen et al.[182]

The ALD system used in this research is Savannah S200, which mainly consists of a reaction chamber, gas lines, pumping system, heating system, control system, precursor cylinders and the ALD manifold as Figure 3-4 shows. Various high-κ

dielectrics like Al_2O_3, HfO_2, and TiO_2 can be grown in this ALD by using trimethylaluminum (TMA), tetrakis(dimethylamino)hafnium (TDMAH), and tetrakis(dimethylamino)titanium (TDMAT) as metal precursors, respectively. H_2O is a commonly used oxidant precursor. The reaction chamber is normally operated in the range of 120 ~ 250°C, and the manifold and exhaust lines should be maintained at 150°C to avoid any condensation. With 20 sccm N_2 introduced in the system, the chamber pressure is around 0.4 Torr. Since the fastest time the ALD valve in this system can fire is roughly 0.015 s, and this is the minimum duration of each pulse. For TMA and other high vapour pressure precursor, the pulse time should be less than 0.02 s. The precursor pulse height should be about 1 Torr or less than the base pressure to prevent premature contamination of the system.

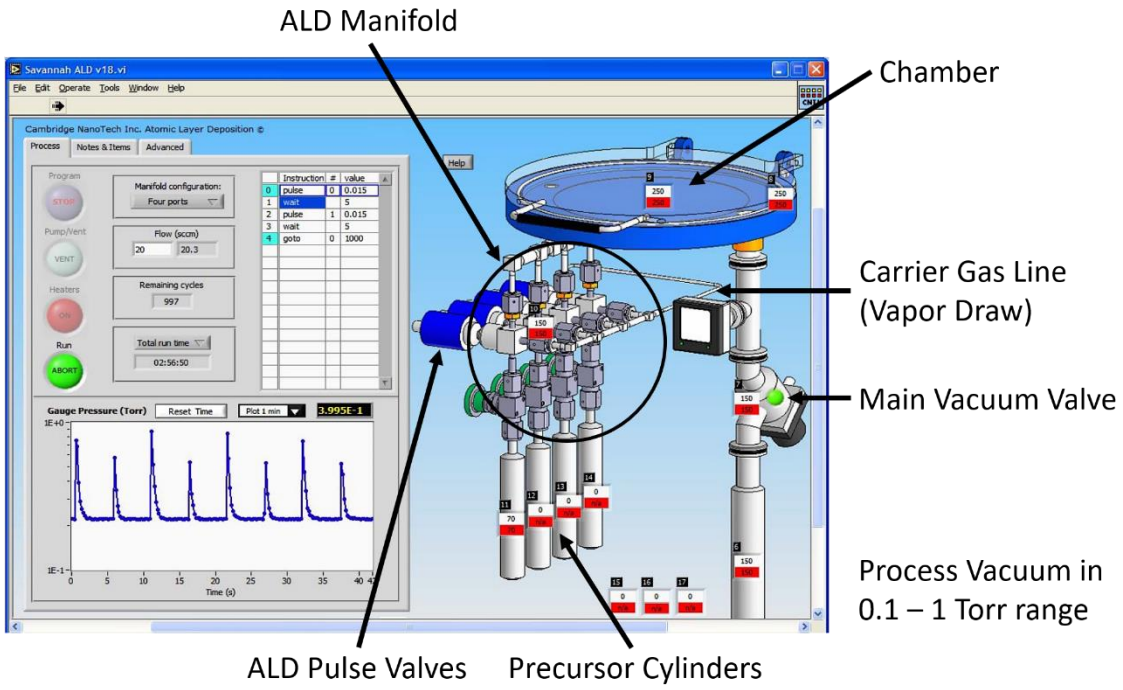

Figure 3-4 Operation interface of Savannah S200 ALD system.

3.3 Transfer Methods

3.3.1 Graphene Transfer

The first necessary step for using the metal-catalysed CVD graphene in device fabrications is to transfer graphene from the metal catalyst like Cu onto a device-compatible substrate like an insulator. An ideal transfer should be able to obtain clean (without contamination) and continuous (without folds, cracks, or holes) graphene film.[184] The graphene transfer method in this research is the commonly used PMMA-

mediated wet transfer.[34,184] Figure 3-5 shows the transfer processes in brief. The CVD graphene/Cu sample is first spin-coated with a layer of PMMA 950 A4 at 5000 rpm for 40 seconds and dried at room temperature for 12 hours. This PMMA layer can protect graphene from damages in the following steps. As graphene can be grown on both sides of the copper, a mild oxygen plasma etching is necessary to remove the graphene on the back side, otherwise it will hinder the Cu etch process. The copper foil is etched away using 0.05M aqueous ammonia persulfate solution (APS, $(NH_4)_2S_2O_8$), and the transparent PMMA/graphene stack floats on the APS solution surface. Typically, it takes about 4 to 5 hours for the 25 µm thick Cu foil to be completely dissolved in the 0.05M APS solution. In order to minimum the contaminations from the oxidized metal particulates introduced by the etchant, the time of rinsing in APS solution should be carefully monitored and once the etching finishes, the PMMA/graphene should be moved out from the etchant to de-ionized (DI) water. Fresh DI water clean for three times with at least 30 min per rinse can effectively remove the Cu contamination remaining after Cu foil etching.[184] Then the PMMA/graphene stack is transferred onto the target substrate and dried at room temperature for 12 hours. Finally, the dried sample is rinsed in acetone to dissolve PMMA for 12 hours, then transferred into isopropyl alcohol (IPA) for a short rinse to remove acetone and dried with N_2. The sample with a graphene film on the target substrate is ready for the device fabrications.

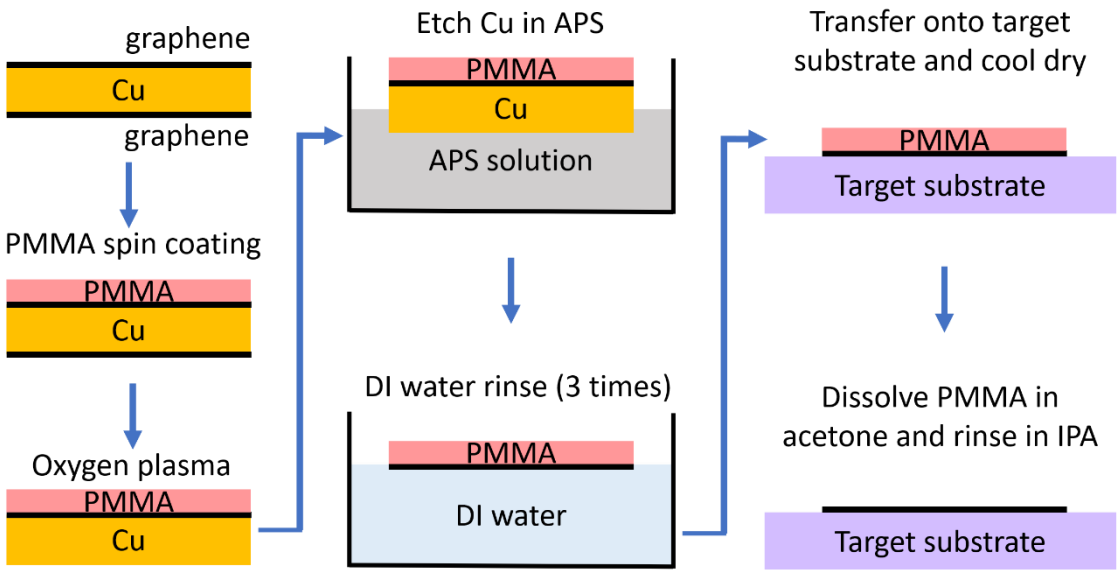

Figure 3-5 Schematic diagram of the graphene wet transfer processes using PMMA as a supporting layer and APS as the Cu etchant.

3.3.2 TMDs Transfer

High-quality TMD flakes are first mechanically exfoliated from a bulk crystal (purchased from 2D Semiconductors, Inc.) with scotch tape (3M, Magic Brand), subsequently transferred from scotch tape onto a PDMS stamp. Then the PDMS supported TMD flakes are transferred onto a target substrate and use fingers to press the stamp against the substrate. Finally, peel off the PMMA stamp very slowly and the TMD flakes have been successfully transferred onto the target substrate. Before the transfer, the target substrate is cleaned in acetone/IPA rinse, and then pre-treated and activated by a O_2 plasma etching for 1 min to remove the dirt and chemical contamination. PDMS stamp is prepared using a mixed solution of the base and curing agent (Sylgard 184, Dow Corning) with a 10:1 volume ratio. Then the mixture is poured onto a clean petri dish and placed in a vacuum desiccator for 1 hour to remove the trapped-air bubbles. The curing can occur by heating on a hot plate in air atmosphere at 100°C for 45 min or leaving at room temperature for 48 hours. PDMS stamp is chosen in the secondary transfer owing to its much lower surface energy (hydrophobic) than those of most substrates like SiO_2, Al_2O_3, and glass etc.[185] Thus, the TMD flakes can easily be detached from PDMS to the target substrate. This all-dry transfer procedure is shown in Figure 3-6. This transfer method can avoid the residues and contamination from the scotch tape and obtained thin TMD flakes large enough for the following device fabrication.

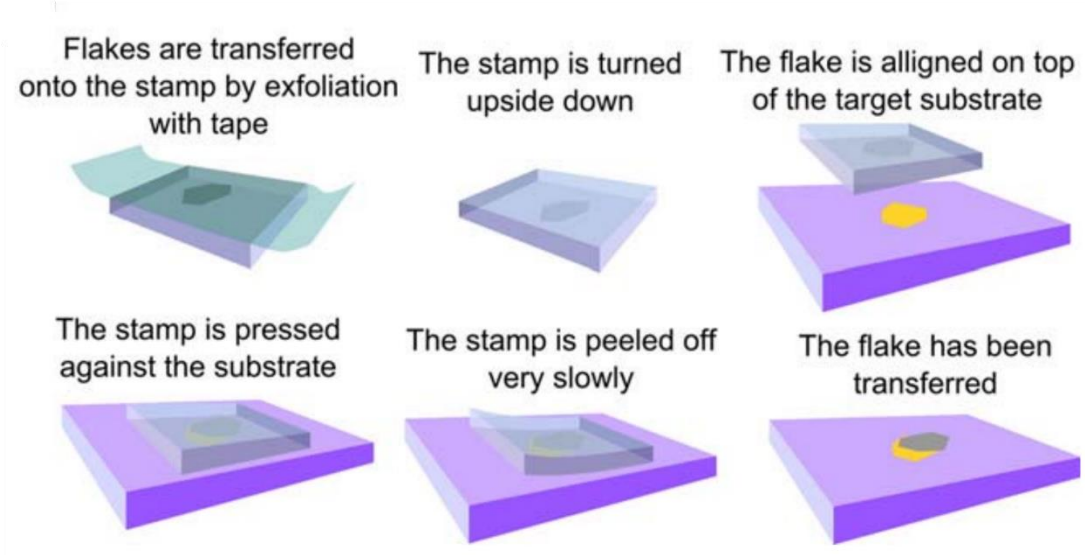

Figure 3-6 Schematic diagram of the all-dry transfer procedure of TMDs using PDMS stamp and scotch tape. ***Figure from Castellanos-Gomez et al.***[186]

3.4 Device Fabrication Techniques

Device fabrication includes electron-beam lithography, material deposition and lift-off. Detailed procedure can refer to Appendix.

3.4.1 Electron-Beam Lithography

Electron-beam lithography (EBL) is to draw custom pattern on a surface covered with an electron-sensitive resist using a focused beam of electrons. The electron beam can change the properties of the resist, and it will become removed (positive resist) or insoluble (negative resist) during the developing step. The great advantage of EBL is that the resolution of the patterns can scale down to sub-10 nm. Moreover, this maskless method enables the custom designed pattern according to the need, which is very suitable for this situation, as the TMDs are randomly transferred on the substrate, and the pattern needs to be modified each time. The machine used in this research is Nano Beam nB5 in CAPE class-100 clean room. UV1116 and PMMA are the two common resists used in this research.

3.4.2 Thermal Evaporation

Thermal evaporation is a widely used method for thin film deposition. The desired material is heated up to the evaporation points in vacuum, and if the vacuum is high enough, the evaporated particles reach the target sample without any collisions and contaminations. Especially in the case of the metal deposition, the high vacuum can ensure the minimal amount of residual oxygen that will result in the deposition of oxides instead. The Blue evaporator in CAPE class-10000 clean room is used for the metal deposition of electrodes in devices.

3.5 Characterization Techniques

3.5.1 Scanning Electron Microscopy

Scanning electron microscopy (SEM) is a powerful tool to observe the topographical, morphological, and composition information of materials. A focused beam of high-energy electrons interacts with atoms in the specimen, generating the secondary and backscattered electrons that can be collected by the electron detectors to produce images of the surfaces. The resolution of SEM depends on the size of the electron spot and the interaction volume and can be in the range of 1 nm to 20 nm depending on the instrument. SEM can provide a quick and non-invasive way to obtain

images of high resolution, high contrast and high surface sensitivity, which make it suitable to investigate the surface features of CVD graphene such as the wrinkles, folding lines, defects, numbers of layers, and wet transfer residues.[187,188]

In general SEM imaging, specimens must be electrically conductive, because nonconductive specimens tend to charge when scanned by the electron beam. This phenomenon can be used to quickly determine whether the CVD graphene has been successfully grown or not because the surface charge can be largely improved with conductive graphene covering the insulting substrates. Due to the atomic thickness of graphene, a relatively low acceleration voltage (~ 1 kV) should be used because high energy electrons could easily penetrate atomically thin materials like graphene and TMDs. Moreover, in-lens detector is preferred because it collects the secondary electrons generated near the incident beam's impact point, which is the major electron-sample interaction volume comes from the surface of atomically thin graphene.

The Carl Zeiss ∑IGMA SEM has been mainly used in this research. The acceleration voltage is maintained at a relatively low value of ~ 1 kV and the working distance is kept at ~ 3 mm.

3.5.2 Optical Microscopy

Optical microscopy (OM, Nikon ECLIPSE LV150N) can quickly magnify images of various specimens *via* the uses visible light and a system of lenses. The magnification in this OM is in the ranges from 5× to 100×, and due to the optical diffraction limit, the best resolution (*d*) for an OM can be reached around 200 nm. This is extracted using the expression $d = \lambda / 2NA$ by assuming that a wavelength of light (λ) is 550 nm, the highest practical numerical aperture (NA) is 0.95 with air and 1.5 with oil. The specimens involve the CVD graphene grown on insulating substrates, the transferred graphene onto other 2D flakes or substrates, and the device structures.

3.5.3 Atomic Force Microscopy

Atomic force microscopy (AFM) is an important instrument capable of imaging specimens with a lateral resolution of ~ 30 nm and a vertical resolution of 0.1 nm, which is 1000 times better than that of the OM.[189] AFM operates by scanning a very sharp tip probe along the sample surface, measuring the force between a probe and the sample to obtain the topography images of the surface. Due to its high surface sensitivity, AFM is a quick and easy method to check the thickness of atomically thin

materials like graphene, few layer graphite, and TMDs. The thickness of single-layer graphene is in the range of 0.8 nm to 1 nm,[1,27,190] and it is from 0.74 nm to 1 nm for WS_2,[169,177,191] and the number of layers can be obtained by measuring the thickness of these 2D materials. The tapping mode is chosen for the measurement, as it can provide higher resolution with minimum sample damages compared to non-contact mode and contact mode. The AFM used in this research is Agilent 5500 in a tapping mode under ambient conditions.

3.5.4 Raman Spectroscopy

Raman spectroscopy can reveal valuable information on the chemical composition, crystalline quality and flake thickness of 2D layered materials from the fingerprint spectra.[192] This technique uses a laser light to interact with a sample, and generates an infinitesimal amount of Raman scattered light that has changed its frequency when interacting with molecular vibrations. To minimize the laser damage to very thin layered materials, the incident laser power must be carefully controlled (within 1% in the following measurements). The choice of laser wavelengths (λ) and microscopy objectives defines the laser spot size for specimens of varied sizes using the expression $1.22\lambda / NA$. The Raman used in this research is Renishaw *InVia* spectrometer. For the direct CVD graphene on insulators, an Ar-ion laser provides Raman signals at 457 nm (200 μW) with a 50× objective (theoretical spot diameter of ~743 nm). For transferred TMDs, a 532 nm laser (400 μW) is used with a 100× objective (theoretical spot diameter of ~721 nm).

3.5.5 X-ray Photoemission Spectroscopy

X-ray Photoemission Spectroscopy (XPS) is a surface characterization technique to analyse the elemental composition, and the chemical and electronic states of materials. XPS spectra are obtained by irradiating a material with a beam of X-rays while the kinetic energy ($K_{kinetic}$) and the number of the emitted electrons are measured. As the energy of an X-ray with particular wavelength is known as $K_{photon} = \hbar\omega_{photon}$, the electron binding energy of the emitted electrons($K_{binding}$) can be determined by $K_{binding} = K_{photon} - (K_{kinetic} + \phi)$, where ϕ is the work function dependent on the spectrometer and the material that can be treated as a constant in practice. Therefore, the kinetic energy carries information regarding the bond energy of electrons can be obtained, which are the fingerprints of elements and their bonding states. The XPS used

in this research is ULVAC PHI Quantera II with a monochromatized Al Kα X-ray source scanning a spot size of 50 μm.

3.5.6 Spectroscopic Ellipsometer

Ellipsometer can provide non-contact thickness and refractive index measurements of thin films to sub-angstrom precision. The basic principle is to use a detector measure the change of polarization of light signal, yielding signal dependence information such as thickness and material properties. The Gaertner L117 ellipsometer is used to measure the thickness of the ALD dielectrics in this research.

3.5.7 Electrical Properties Measurements

Electrical properties of all the devices are characterized by a standard four-probe method (Keithley 4200-SCS Semiconductor Characterization System) in ambient atmosphere at room temperature. Current-voltage curves for diodes, transfer curves and output curves for field-effect transistors are measured in this research.

4 METAL-CATALYST-FREE CVD SYNTHESIS OF GRAPHENE ON INSULATORS

In this chapter, the metal-catalyst-free growth of uniform and continuous graphene films on different insulating substrates was investigated by microwave PECVD with a gas mixture of C_2H_2, NH_3, and H_2 at relatively low temperature of 700 ~ 750°C. Compared to growth using only C_2H_2 and H_2, the use of NH_3 during synthesis is found to be beneficial, in transforming vertical graphene nano-walls into a layer-by-layer film, reducing the density of defects, and improving the graphene quality. The effect of different insulating substrates (including Al_2O_3 and SiO_2) on the growth of graphene was studied under different growth temperatures, implying the growth-temperature window and catalytic effect vary among insulators. The low activation energy barrier of Al_2O_3 proves it to be a more suitable substrate for the metal-catalyst-free growth of graphene at low temperature. These directly grown graphene films on insulators can be conveniently integrated into various electronic and optoelectronic applications avoiding any post-growth transfer process.

4.1 Introduction

Graphene is a single layer of sp^2-bonded carbon atoms packed into a honeycomb lattice. It has been regarded as one of the most attractive candidates for future electrical and optical applications owing to its excellent properties such as high carrier mobility, optical transparency, mechanical flexibility, and high thermal conductivity.[1,44] To fully realize its potential in real-world devices, metal-catalyst CVD has been widely used in the large-scale, high-quality and cost-effective synthesis of graphene. However, this method has significant limitations in that the growth is normally carried out at ~ 1000°C,[28,29,34,193–195] on a metal catalyst and requires a post-growth transfer process from metal onto an insulating substrate to make the device. The difficult transfer process usually results in polymer or metal residues, and wrinkling or breakage of graphene.[26,46,196] Therefore, it would be a great advantage to develop a direct, metal-catalyst-free growth method of graphene onto insulating substrates at low temperature.

Unfortunately, insulating substrates generally display weak catalytic nature. The principle role of the catalyst in graphene growth is to dehydrogenate the precursor species[197] and to chemisorb the hydrocarbon as a mobile surface species to cluster into the growing graphene grains. Some oxides such as VO_x and Cr_2O_3 can act as dehydrogenation catalysts. The stability of strongly bonded oxides such as ZrO_2 or HfO_2 against reduction by carbon and have been used to grow carbon nano structures.[78,79,198,199] There is also the novel idea of using remote copper or iron based catalysts which are then volatilized after the graphene growth.[57] Nevertheless, the direct growth of graphene onto insulating substrates has been frequently tried and tends to show degraded quality compared with those grown on metals.[200] In order to overcome the large energy barrier for graphene nucleation without metal catalysts,[201] even higher temperatures (1065 ~ 1650°C) are required by thermal CVD to obtain graphene to compete with the metal-catalysed growth.[63,68,77,202,203]

To lower the growth temperature, it is useful to consider PECVD method with the assist from plasma.[204] The presence of energetic electrons, excited molecules/atoms, and free radicals generated in the plasma region can promote the decomposition of reactant gases, thus partly compensating for the weak catalytic nature of insulating substrates.[205] Several PECVD studies have been reported on SiO_2,[88–99] quartz,[88,91,94] glass,[97,100] and Al_2O_3[89,91] to explore the synthesizing graphene without metal catalysts at low temperature. Successful enlargement of isolated grain sizes has been realized using two-step growth in PECVD process.[88,89,92,93] However, extremely long growth times (over

9 hours)[88] or high-temperature pre-annealing (1000°C)[92] was still needed to obtain isolated grains, and high mobility values were only measured on single grain devices due to discontinuous films.[89,92,93] Other groups tried to grow continuous graphene using PECVD. However, these films suffered from common problems such as many defects, less surface uniformity,[90,91,94–100] and 3D nano-wall growth.[90,94,97,101] All these drawbacks have limited graphene from fulfilling its excellent electrical properties and developing its advantage of atomic thickness. Therefore, a continuous, uniform, and 2D graphene film with a low defect density is desirable, which can enable graphene integrated with the modern silicon electronics as well as other 2D materials like transition metal dichalcogenides.

When it comes to device fabrication, insulators serve as gates in field effect transistors (FETs), which have a strong influence on fulfilling the properties of graphene. However, the weak catalysis of insulators makes the selection of more proper insulating substrate essential in the metal-catalyst-free growth of graphene. SiO_2 might not be an ideal substrate for graphene FETs, because the high interface states density and impurity-induced trapped charges on SiO_2 substrates could cause carrier scattering issues that limit the performance of devices.[206] Recent studies suggest that using high dielectric constant (high-κ) materials like Al_2O_3 as gate insulators would boost the performance of devices due to the reduction of Coulomb scattering in graphene owing to the dielectric screening effect.[207] Therefore, the direct assembly of graphene on high-κ dielectrics would be useful. ALD is a typical technique to obtain high-quality, thickness-controlled, pinhole-free high-κ thin films, which could provide a smooth and continuous surface for the graphene growth.[208] Furthermore, the graphene/high-κ dielectric structure could be easily applied onto any semiconductor or substrate for functional device fabrications. However, the only attempt of metal-catalyst-free PECVD growth of graphene on atomic layer deposited Al_2O_3 substrates[91] faced all the common problems mentioned above such as a high density of defects and multi-layer structures, but factors that degraded the quality and the mechanism behind it are not very clear.

In this chapter, the metal-catalyst-free growth of graphene on SiO_2 and Al_2O_3 by PECVD has been realized to investigate the practical solutions to reduce the density of defects and 3D nano-walls. By decreasing the concentration of the carbon gas and especially introducing NH_3 in the growth, continuous and uniform graphene film with a low density of defects and no 3D nano-walls can be synthesized in the microwave PECVD system, thus the quality of graphene has been improved. Moreover, the

graphene films produced on SiO_2 and Al_2O_3 under different growth temperatures have been compared, which can offer a better understanding of the weak catalytic effect of different insulating substrates on the graphene growth.

4.2 Experimental Methods

4.2.1 Preparation of Insulating Substrates

High-κ dielectrics were deposited on SiO_2 (300 nm)/p-Si wafer using ALD. Before the ALD process, all the wafers were cleaned by sonication in acetone, IPA, and DI water, and then dried with N_2. The cleaned wafers were placed in the chamber of Savannah S200 ALD reactor at the temperature of 200°C with 20 sccm N_2 introduced as both carrier gas and purge gas, and the chamber pressure is around 0.4 Torr. H_2O was used as the oxidant precursor. TMA, TDMAH, and TMDAT were used as metal precursors to deposit Al_2O_3, HfO_2, and TiO_2, respectively. TDMAH and TDMAT as solid precursors, should be heated up to 75°C to be vaporized as vapour-phase precursors for ALD process while TMA as a liquid high vapour pressure precursor, can be vaporized at room temperature.

The deposition rates for Al_2O_3, HfO_2, and TiO_2 using these recipes are 0.105 nm/cycle, 0.101 nm/cycle, and 0.05 nm/cycle. By changing the number of growth cycles, high-κ thin film was obtained with thicknesses of 3 nm measured by ellipsometry. Besides Al_2O_3, SiO_2 (300 nm)/p-Si substrates were used as the control group in the graphene growth. Other insulating substrates were also tested in experiments to investigate the effect of insulating substrates on the graphene growth, including sapphire, quartz, MnO_2 spin-coated on SiO_2 substrates.

4.2.2 Growth of Graphene by Microwave PECVD

The low-temperature growth of graphene on various insulators was carried out in a homemade microwave (2.45 GHz) PECVD system using reactant gases including CH_4 or C_2H_2, NH_3, and H_2, as schematically shown in Figure 4-1a. Dielectric substrates were placed on a Pyrolytic Boron Nitride/Pyrolytic Graphite heater element enclosed in a metal cage with a honeycomb mesh shield, as shown in the zoom-in image (Figure 4-1b). This configuration can protect the samples from the ion-induced damage of the plasma ball, while the energetic and reactive species could pass through the mesh shield and reach the substrates to synthesize graphene. First, insulating substrates were heated to 650 ~ 800°C after pumping down the chamber to 1×10^{-6} mbar. Second, H_2

was introduced at a rate of 400 sccm and a microwave plasma was ignited above the metal cage at a pressure of 15 mbar and a power of 600 W for 10 min. Third, a gaseous carbon source (CH_4 or C_2H_2) with/without NH_3 were added to the H_2 flow to start the graphene growth. The total gas flow rate was kept at 400 sccm (CH_4: 10 ~ 40 sccm, C_2H_2: 20 ~ 40 sccm, NH_3: 0 ~ 120 sccm, and H_2: 240 ~ 390 sccm). Finally, after four-hour growth (three-hour if the carbon source is C_2H_2), samples were cooled down by switching off the CH_4 or C_2H_2 and NH_3 flow, the plasma, and the heater power supply.

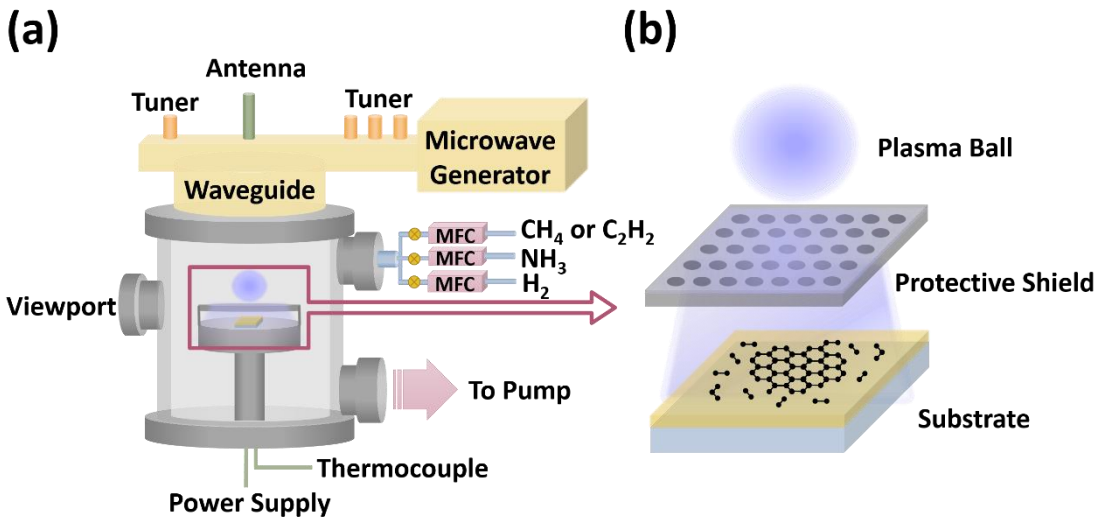

Figure 4-1 Schematic illustrations of (a) the homemade microwave PECVD system and (b) the zoom-in image of the graphene growth process.

4.2.3 Device Fabrication

The as-grown graphene is ready for device fabrications without any post-transfer process. The whole fabrication involves EBL, oxygen plasma etching, metal deposition, and lift-off technology. Two-step lithography is used to define electrodes and registration marks for the alignment (layer 1) and pattern graphene areas (layer 2). For a 1×1 cm^2 chip, it contains 100 devices for EBL as the mask is shown in Figure 4-2a. UV1116 or PMMA 950 A8 can be both used as photoresist. 5 nm Cr/50 nm Au is deposited by thermal evaporator (homemade Blue Evaporator in CAPE) and then the sample is rinsed in acetone with a few drops of IPA solution overnight for the metal lift-off. After the second EBL to define the graphene area, extra graphene is etched away by O_2 plasma in Reactive Ion Etching system (Philip RIE). The photoresist is removed by acetone/IPA and then the chip is gently dried with N_2. The OM images of the chip and the zoom-in image of a single device are shown in Figure 4-2b&d, and the schematic

image of the device for four-probe measurement is illustrated in Figure 4-2c. The width of the graphene stripe is 5 μm and the distance between electrodes is 2 μm.

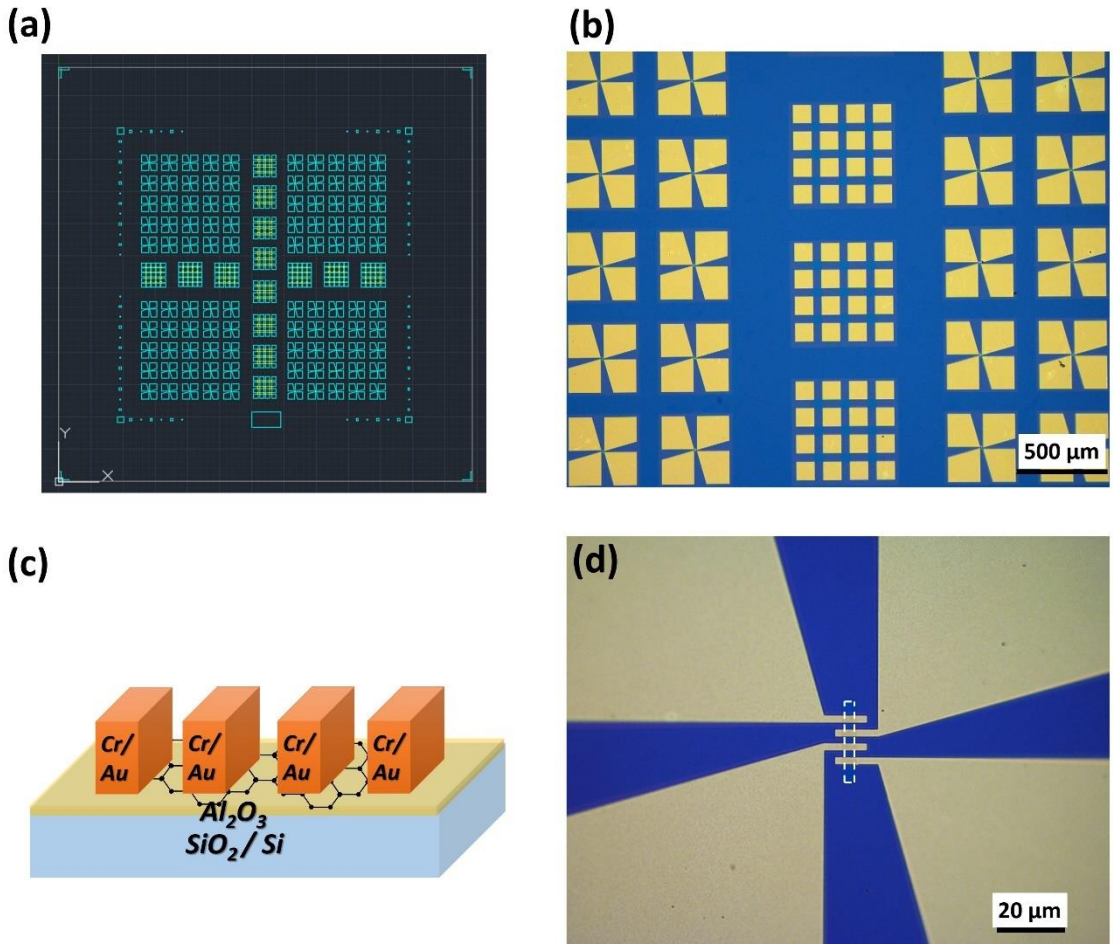

Figure 4-2 (a) Pattern for two-step lithography. (b) OM images of the device array with 5 nm Cr/50 nm Au as electrodes. (c) Schematic illustration of a device structure for four-probe measurements. (d) OM image of a single device.

4.3 Optimization of Metal-Catalyst-Free Growth of Graphene

4.3.1 Effect of Carbon Precursors

Methane (CH_4), ethylene (C_2H_4), and acetylene (C_2H_2) are widely used gaseous carbon precursors for graphene synthesis.

In previous study of the graphene growth on Cu, CH_4 as a carbon source is strongly affected by hydrogen, which acts as an activator of the surface bound carbon to form the monolayer graphene, and an etching reagent that controls the size and morphology of the graphene domains.[209] In the study of graphene synthesis on insulating substrates, it has been reported that the CH_4/H_2 ratio plays a very important role in the CVD graphene growth.[74,80,100]

To investigate the effect of CH_4/H_2 ratio on the growth of graphene on insulating substrates, the total flow rate of CH_4/H_2 mixture has been fixed into 400 sccm. By only changing the flow rate of CH_4 from 10 sccm to 45 sccm, different samples can be obtained under various CH_4/H_2 ratios. The growth temperature is 800°C and the growth time is 4 hours. Figure 4-3 shows the SEM images of the as-grown graphene on SiO_2 (a-e) and Al_2O_3 (f-j) substrates with the increase of CH_4/H_2 ratios. The layer-by-layer graphene flakes could be synthesized at the CH_4/H_2 ratio of 40:360 sccm, which is the best CH_4/H_2 ratio for the graphene growth in this experimental setup.

The amount of hydrogen is critical to the growth of graphene, since hydrogen balances the production of reactive hydrocarbon radicals and etching effect of graphite during CVD.[74] If the ratio of hydrogen is too high in the reaction, such as results of the CH_4/H_2 ratio of 10:390 sccm in Figure 4-3a&f, etching becomes the dominant process in the CVD reaction, resulting in graphene with many defects and disorder or even no graphene on insulating substrates. If the ratio of hydrogen is a little lower in the reaction, like the results of the CH_4/H_2 ratio of 45:355 sccm in Figure 4-3e&j, nucleation becomes the dominant process, leading to a large number of graphitic clusters covering the whole surface. At the very high ratio of CH_4 (such as 80 sccm), the surfaces are not smooth or flat, because some graphene sheets were grown vertically and randomly oriented on the substrates to form three-dimensional structures. This phenomenon has also been reported in previous work.[65,97] Therefore, the CH_4/H_2 ratios for crystal growth of graphene are located in a very narrow growth window.

Figure 4-4 is the zoom-in SEM images and the corresponding AFM images at the best CH_4/H_2 ratio. The thicknesses measured from the AFM images are about 1 nm, which can further confirm monolayer graphene has been grown on Al_2O_3 and SiO_2 substrates.

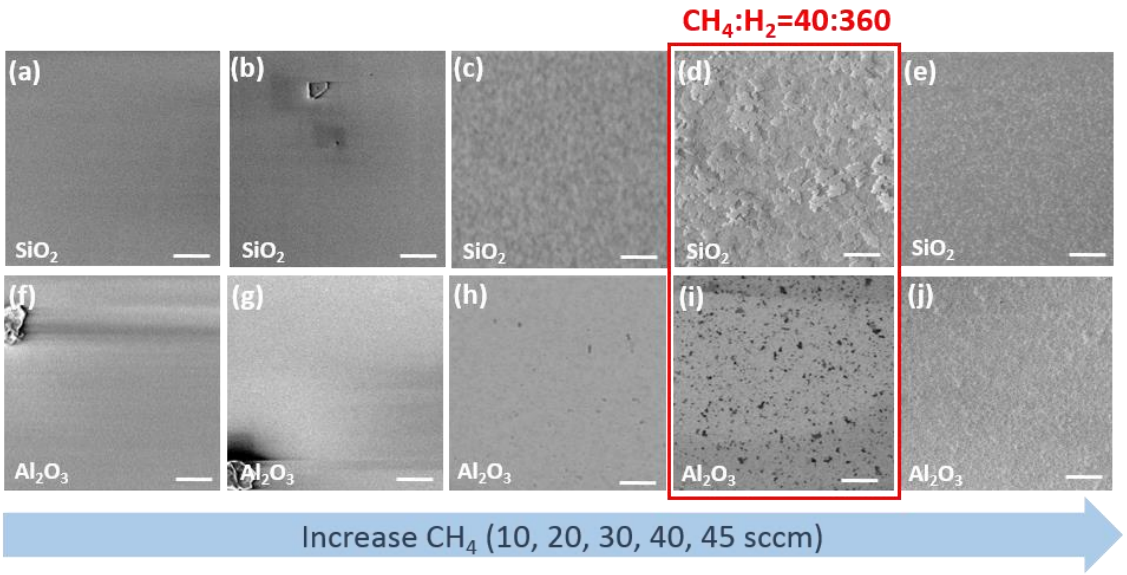

Figure 4-3 SEM images of graphene grown directly on SiO_2 (a-e) and Al_2O_3 (f-j) at 800˚C for 4 hours by microwave PECVD using CH_4 + H_2, respectively. The CH_4 flow rate increases from 10 to 45 sccm in the direction of arrow. The scale bars are 1 μm.

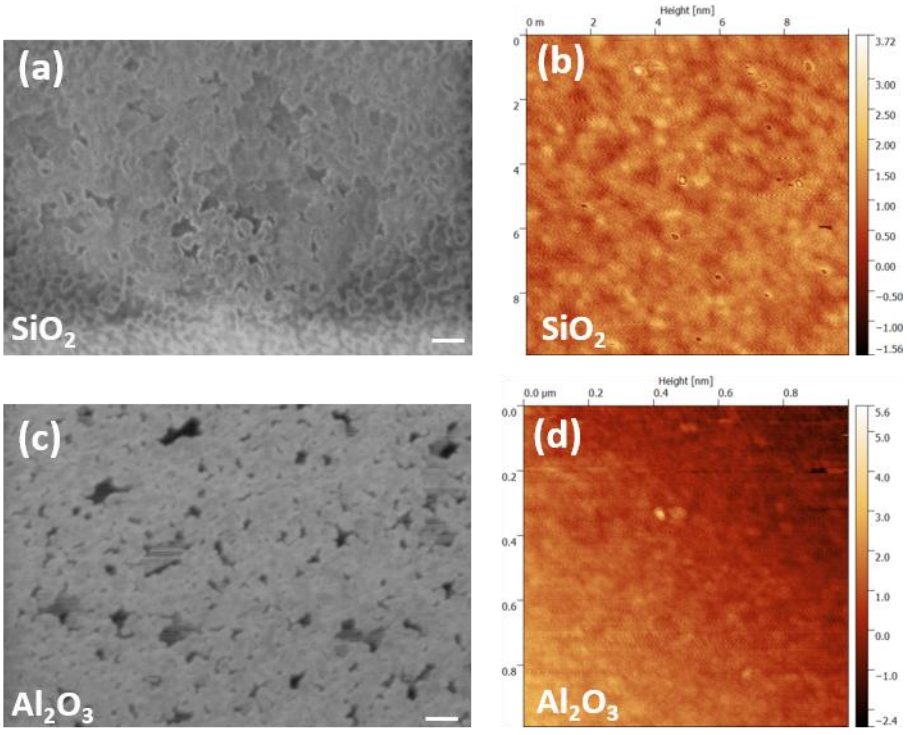

Figure 4-4 Zoom-in SEM images of graphene grown on (a) SiO_2 and (c) Al_2O_3 substrates with the CH_4:H_2 ratio of 40:360 (sccm). The scale bars are 200 nm. The corresponding AFM images of samples on (b) SiO_2 and (d) Al_2O_3 substrates, respectively. The measured area is 1×1 um^2.

Figure 4-5 depicts the corresponding Raman spectra of the graphene grown on SiO_2 and Al_2O_3 substrates by varying the CH_4/H_2 ratios. The D peak, G peak, and 2D peak, centred at around 1370, 1580, and 2700 cm^{-1} respectively, are the predominant features in each Raman spectrum.[210] The 2D peak is a second-order two-phonon process related to a phonon near the K point in graphene, corresponds to the dispersive nature, and strongly depends on any perturbation to the electronic and/or phonon structure of graphene, therefore the 2D peak is regarded as the signature of graphene to differentiate itself from other sp^2 nanocarbons.[211] The G peak is caused by the stretching of the C-C bond in graphitic materials and is common in all sp^2 carbon system. The G peak is highly sensitive to strain effects in sp^2 nanocarbons and can be used to characterize the strain induced by external force, such as the strain caused between graphene layers in the case of few layer graphene.[211] The D peak is caused by the disorder in the sp^2 hybridized carbon atoms and can be observed where symmetry is broken by edges or in samples with a high density of defects. So, the D peak can provide very important information about the disorder and defects in sp^2 carbon materials. In order to compare the intensities of G peaks and 2D peaks among different samples, all the D peaks in this work's Raman spectra were normalized.

As the CH_4/H_2 ratio changes from 40:360 (sccm) to 10:390 (sccm), the full width at half maximum (FWHM) of the 2D peak increases gradually and the intensity ratio of I_{2D} to I_G decreases gradually. In the case of Al_2O_3 substrates, the FWHM of the 2D peak increases from 41 cm^{-1} to 69.2 cm^{-1}, and the intensity ratio I_{2D}/I_G decreases from 1.21 to 0.42. As for SiO_2 substrates, the FWHM of the 2D peak increases from 65 cm^{-1} to 85 cm^{-1} and the intensity ratio I_{2D}/I_G decreases from 0.57 to 0.38. So, by changing the CH_4/H_2 ratios changes from 40:360 (sccm) to 10:390 (sccm), the quality of graphene decreases, as a sharp and high 2D peak is highly desirable. Another feature from the Raman spectra is the very high intensity ratio I_D/I_G and the sub-peak of G band, which is called D' peak. Even for the best results, I_D/I_G is 1.70 and 2.47 for graphene synthesized on SiO_2 and Al_2O_3 substrates. The D' peak is defect-induced, and arises from the intravalley double-resonance process.[212] D peak and D' peak appear when graphene is damaged, and can be regards as a sensitive and informative signal to characterize disorder and defect in graphene.[211,213]

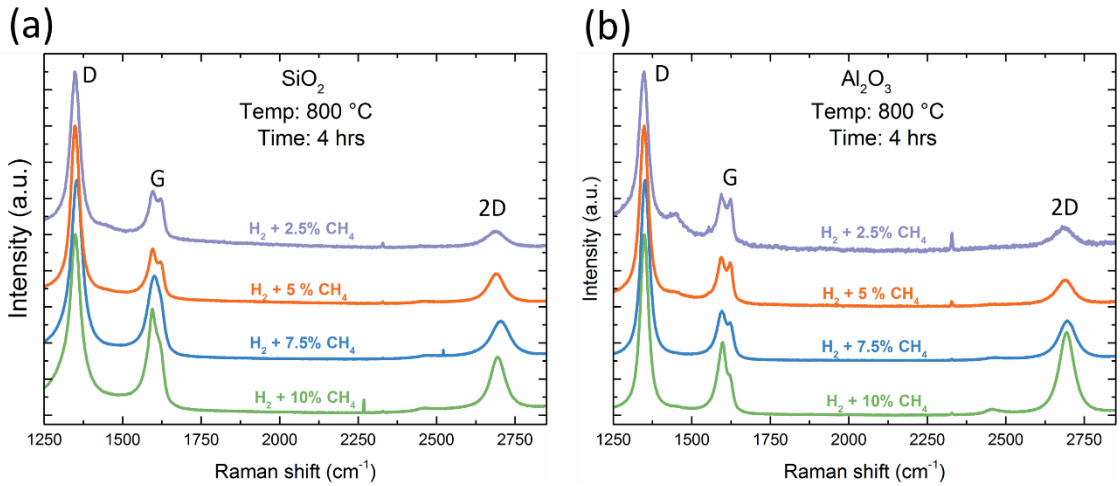

Figure 4-5 Raman spectra of graphene films deposited on (a) SiO_2 and (b) Al_2O_3 substrates at different CH_4/H_2 ratios. The CH_4/H_2 ratio varies from 40/360 sccm to 10/390 sccm. The growth temperature is 800°C and the growth time is 4 hours.

Apart from the high density of defects, the chemical reaction took place at the temperature of 800°C, which is relatively high for the large-scale production and integration with current silicon technologies. To study the potential of CH_4 to promote reactions at low temperature, the growth temperature decreased from 800°C to 700°C, and the SEM images of as-grown graphene samples on Al_2O_3 substrates are shown in Figure 4-6. It was found the coverage of graphene film was reduced with the decrease of the growth temperature, implying the temperature of 700°C is unable to offer enough energy for the reaction.

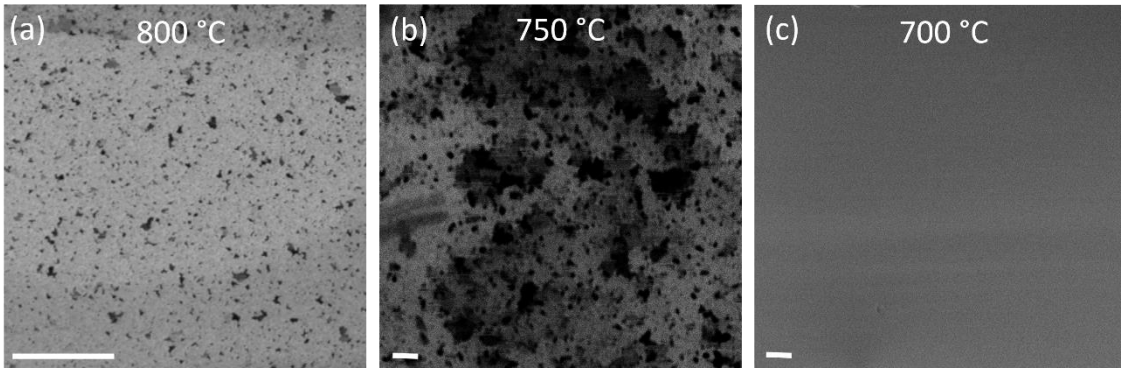

Figure 4-6 SEM images of sample surfaces after synthesis under the CH_4:H_2 ratio of 40:360 (sccm) at various growth temperatures on Al_2O_3 substrates. The coverage of graphene was reduced when decreasing the temperature and (c) no graphene was produced at 700°C. The scale bars are 2 μm.

C_2H_2 is a promising carbon precursor for the low-temperature CVD synthesis of graphene. The early use of C_2H_2 for the CVD growth of CNTs has demonstrated its

ability to reduce the temperature to 350°C.[214] Later it has been used in the CVD growth of graphene on metal catalysts like Ni.[215] The reason why graphene can be synthesized at lower growth temperature with C_2H_2 other than CH_4 can be attributed to the lower barrier energy for breaking the C-C bond than for the C-H bond on the Ni surface, which results in lower dissociation temperature of C_2H_2.[216] Several groups reported that using C_2H_2 can realize the metal-catalyst-free growth of graphene at lower temperature,[78,79,89,92] and the lowest growth temperature achieved so far is 325°C.[78] In a PECVD setup, the competition between the effects of H_2 plasma etching and C_2H_2 decomposition can be expressed by the following equilibrium:[92]

$$C_2H_2(s) \underset{\text{etching}}{\overset{\text{growth}}{\rightleftharpoons}} \text{graphene}(s) + H_2(g) - Q \qquad (4\text{-}1)$$

where Q is heat. Accordingly a high H_2 content or low temperature will cause edge etching, whereas a low H_2 content or high temperature will facilitate the nucleation of small graphitic clusters.[92] Since the hydrogen content of C_2H_2 is lower than that of CH_4, fewer atomic hydrogen will be produced from the precursor itself, which means the critical equilibrium could happen at lower temperature.[89] By replacing CH_4 with C_2H_2, the growth window can be further reduced to 650 ~ 750°C in the experiments, therefore, the following results and discussions will focus on the CVD synthesis of graphene using C_2H_2 as a carbon precursor.

4.3.2 Effect of Ammonia Concentrations

Compared with H_2 plasma, NH_3 plasma has been proved a more effective etching gas in generating atomic hydrogen species.[89,217–219] Control experiments were first conducted to grow graphene in microwave PECVD using only H_2 and C_2H_2, and the growth temperature was 750°C and growth time was 3 hours. It was found that growth of multi-layer graphene commonly appeared on both SiO_2 and Al_2O_3 substrates at high C_2H_2 volume concentrations. However, by decreasing the concentration of C_2H_2 from 10% to 5%, 3D nano-walls could be greatly reduced on both substrates as shown in the left column (the blue area) in Figure 4-7. PECVD assisted growth of graphene can be regarded as the competing result of graphene nucleation and growth due to the saturation of hydrocarbon precursors and the etching of carbon by atomic hydrogen. The abundant carbon source results in repeated nucleation and vertical growth under an insufficient H_2 situation, which can be improved by reducing the concentration of carbon source to avoid excess carbon or increase the concentration of H_2 to gain a strong etching effect.[92,220,221]

To investigate the effect of NH_3 on the growth of graphene, we intentionally kept the C_2H_2 concentration at a high level of 10%, which would lead to 3D nano-wall growth of graphene using C_2H_2/H_2 plasma as shown in Figure 4-7c&h. With increasing NH_3 concentration from 0 to 30%, the surface morphology varied on both SiO_2 and Al_2O_3 substrates, as shown in the right column (the yellow area) in Figure 4-7. By replacing 40 sccm H_2 with the same amount of NH_3 (15% NH_3), 3D nano-walls were reduced on both insulating substrates shown in Figure 4-7d&i. By increasing the NH_3 concentration to 30%, layer-by-layer structures were obtained on both insulating substrates shown in Figure 4-7e&j. For the SiO_2 substrate, the growth mode was in a layer-by-layer manner and the whole substrate was covered by graphene flakes. For the Al_2O_3 substrate, a continuous and uniform graphene sheet was directly synthesized on the substrate.

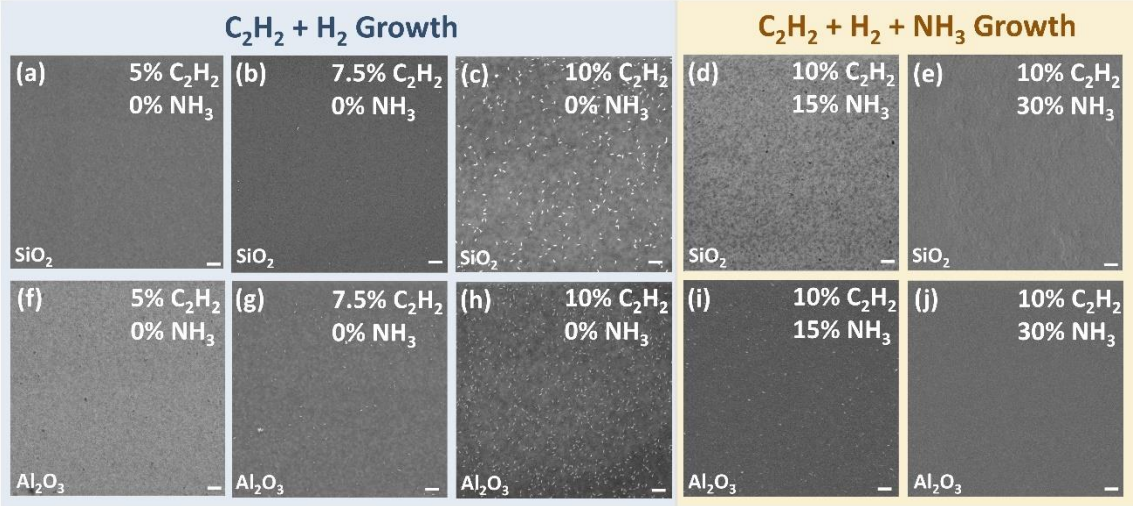

Figure 4-7 SEM images of graphene grown directly on SiO_2 (a-e) and Al_2O_3 (f-j) at 750˚C for 3 hours by microwave PECVD using C_2H_2 + H_2 (left column) and C_2H_2 + H_2 + NH_3 (right column), respectively. The C_2H_2 and NH_3 concentrations are given in the images. The scale bars are 200 nm.

It is also found that further increasing NH_3 will lead to the growth of discontinuous graphene. Wei *et al.* studied the growth of graphene by PECVD using only NH_3 and a carbon source such as C_2H_2, CH_4 or C_2H_4.[89] In their work, the growth temperature and the ratio of NH_3 and hydrocarbon gas were systematically varied to find the optimal growth condition. High-quality graphene with low density of defects has been synthesized using this binary growth. However, only discontinuous graphene domains were produced, which will limit its applications.

Figure 4-8 is the corresponding Raman spectra of the as-grown samples shown in Figure 4-7. The intensity ratio of D peak to G peak (I_D/I_G) can provide important information of the density of defects and the crystallite size of graphene.[222] When evaluating these two methods of reducing 3D nano-walls, the method of introducing NH_3 outweighs the method of decreasing the concentration of carbon source in reducing the density of defects and enlarging the crystallite size of graphene. Graphene grown on both SiO_2 and Al_2O_3 substrates using C_2H_2/H_2 plasma have a common feature that a relatively high density of defects caused by the high fraction of open edges of small crystallite sizes.[222] By introducing NH_3, I_D/I_G on both SiO_2 and Al_2O_3 substrates decreases greatly by 55.6% and 80.8% respectively.

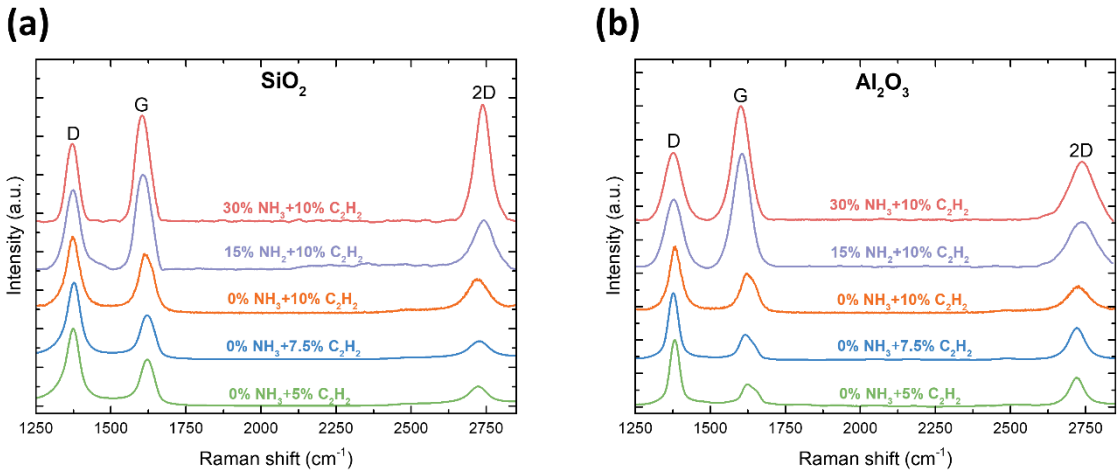

Figure 4-8 Corresponding Raman spectra of the as-grown samples shown in Figure 4-7 in case of SiO_2 substrates and (b) Al_2O_3 substrates.

As I_D/I_G is inversely proportional of the grain size (L_a) for L_a above 2 nm, this can be used to study the level of disorder and assess the graphene quality. It can be also used to estimate the domain sizes (or crystal sizes) using Tuinstra and Koenig relation:

$$L_a\,(\text{nm}) = C(\lambda_l)(I_D/I_G)^{-1} = (2.4 \times 10^{-10})\,\lambda^4\,(I_D/I_G)^{-1} \qquad (4\text{-}2)$$

where λ_l is the excitation laser wavelength, C(457 nm) ~10.47 nm.[223,224] The λ_l^4 power dependence of the I_D/I_G ratio in Equation (4-2) is observed for graphene[213] and nanographite.[224] This is useful to estimate the magnitude of the domain sizes, which are hard to observe in SEM for the nanographene synthesized on insulators. Figure 4-9 also demonstrates the effect of reactant gases on L_a. It can be seen, L_a increases dramatically from 8.18 nm to 14.3 nm for graphene films grown on SiO_2 substrates and from 6.42 nm to 17.8 nm for Al_2O_3 substrates when increasing the NH_3 concentration from 0 to 30%.

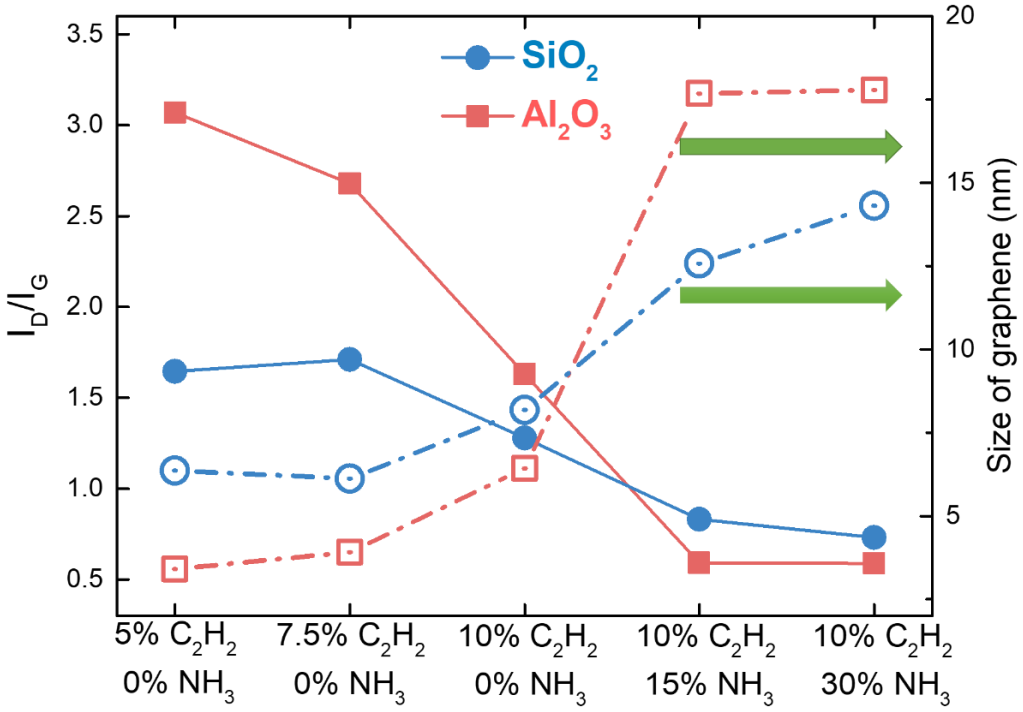

Figure 4-9 The intensity ratios (I_D/I_G, solid symbols and lines) and the sizes of graphene (open symbols and dash dot lines) of the as-grown graphene films under different conditions for three-hour synthesis at 750˚C.

The high sensitivity to the specific sp^2 nanocarbons makes the 2D peak in Raman spectroscopy very useful in distinguishing graphene with different layers.[225] For metal-catalysed CVD graphene, the intensity ratio of 2D peak to G peak (I_{2D}/I_G) ≈ 2 and a single Lorentzian 2D peak with a FWHM of 30 cm^{-1} indicate monolayer graphene, the feature of $1 < I_{2D}/I_G < 2$ with the 2D peak being fitted to four Lorentzian peaks is for bilayer graphene, and the feature of $I_{2D}/I_G < 1$ with the 2D peak being fitted to two Lorentzian peaks suggests multilayer graphene.[29,34,226] However, for metal-catalyst-free CVD graphene, I_{2D}/I_G for monolayer graphene is lower (around 1.2 ~ 1.5) and the FWHM of 2D peak is broader (around 60 cm^{-1}) due to the non-negligible D peak resulting in the breakage of the hexagonal symmetry in graphene.[68,89,227] Among all the samples, the graphene grown on SiO_2 substrate under 30% NH_3 shows that I_{2D}/I_G ~ 1.11 and the FWHM of 2D peak ~ 57.1 cm^{-1}, which implies monolayer graphene have been produced, and it further confirms the layer-by-layer structures observed by SEM in Figure 4-7e. As for Al_2O_3, when increasing the NH_3 concentration from 15% to 30%, I_{2D}/I_G increases from 0.39 to 0.51, which suggests that the as-grown graphene is multilayer, but its layer number reduces with the increase of NH_3. However, by further increasing the NH_3 concentration to 45%, L_a decreases to 7.8 nm (on SiO_2 substrates)

and 9.9 nm (on Al_2O_3 substrates) as shown in Figure 4-10. The quality degradation has been observed, and the reason for that is the structure distortion caused by N-doping will result in large amount of topological defects thus leading to a higher D peak for N-graphene than that of C-graphene.[228] Therefore, owing to the presence of NH_3, and the growth mode turns from vertical graphene nano-walls to layer-by-layer films, and we can conclude that 30% NH_3 is the optical condition in the system to synthesize high-quality graphene with a lower density of defects, larger crystal sizes, and fewer layers for both substrates.

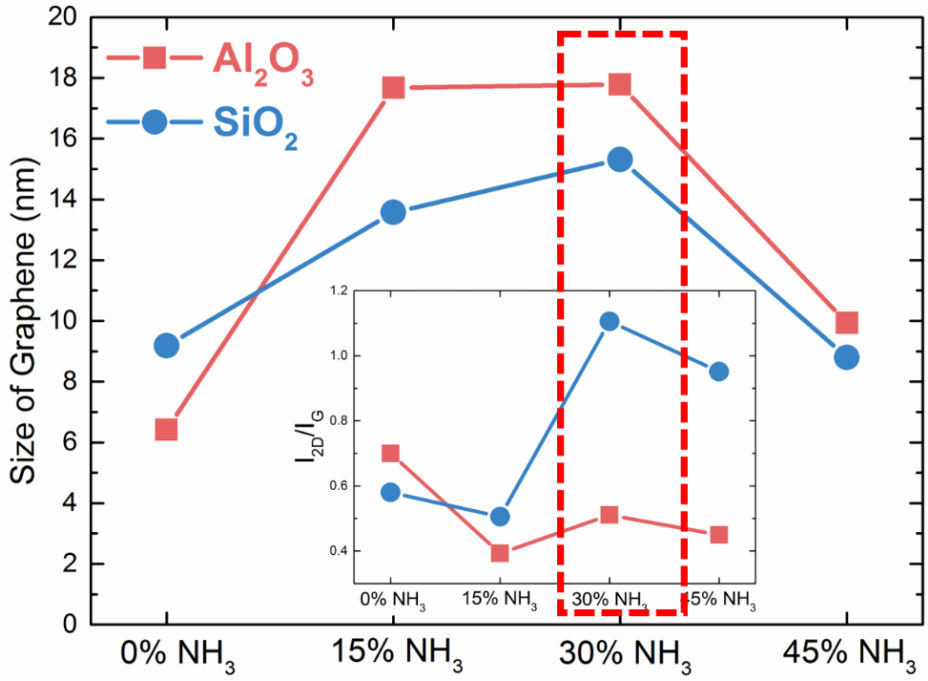

Figure 4-10 Raman spectra of graphene films grown under different NH_3 concentrations. The insets are the intensity ratio of 2D peak to G peak.

Figure 4-11 presents the summery of the intensity ratios (I_D/I_G and I_{2D}/I_G) of graphene synthesized on insulators by PECVD method below 900˚C. The lower region in Figure 4-11 corresponds to graphene with very few defect while the upper region is for graphene with high density of defects. The lower left corner refers to multilayer graphene while the lower right corner is for monolayer graphene. Most PECVD studies suffered from high density of defects and discontinuous growth of graphene as shown in Figure 4-11. Compared to other published work, this work is close to the lower left corner, which means the growth of uniform and continuous multilayer graphene films with the lowest density of defect has been achieved, and Al_2O_3 demonstrates itself as a more competitive and suitable substrate for producing low-defect, large-area, and uniform multilayer graphene in comparison with SiO_2.

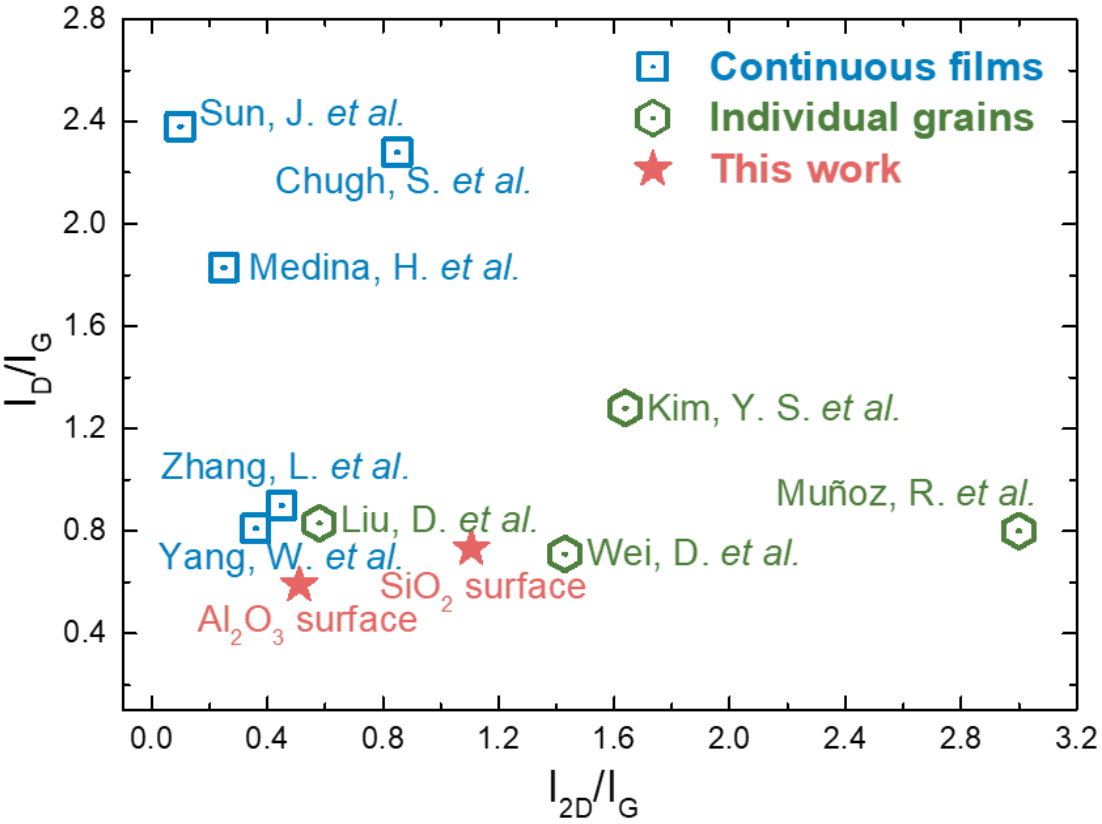

Figure 4-11 A summary of the intensity ratios of I_D/I_G and I_{2D}/I_G of graphene synthesis on insulators by PECVD method. Blue square: continuous films (Sun, J. *et al.*, [95] **Chugh, S. *et al.*,** [94] **Medina, H. *et al.*,** [98] **Zhang, L. *et al.*,**[91] **and Yang, W. *et al.***[99]**); green hexagon: individual grains (Kim, Y. S. *et al.*,**[96] **Liu, D. *et al.*,**[93] **Muñoz, R. *et al.*,**[88] **and Wei, D. *et al.***[89]**); red star: this work.**

4.3.3 Effect of Insulating Substrates

Besides the effect of NH_3 concentration on the growth, the SEM images also indicate insulators influence the surface morphologies of graphene. Under the same NH_3 concentration and temperature, Al_2O_3 substrate favours a more effective nucleation stage and a faster growth stage compared with SiO_2, resulting in either a higher density of 3D graphene nano-walls shown in Figure 4-7c&h or a better coverage on the substrate in Figure 4-7e&j. The reason seems to be the smaller activation barrier of Al_2O_3 in the graphene growth, and such a low energy barrier ensures the dissociative adsorption of C_2H_2 to carbon adatom could happen at low temperature.

To further confirm that, a controlled experiment was conducted on Al_2O_3 substrates under the same growth condition (40 sccm C_2H_2, 120 sccm NH_3, and 240 sccm H_2) by only decreasing the growth temperature from 750˚C to 650˚C. At 750˚C, a uniform and continuous graphene film was produced (Figure 4-12a), and by decreasing the growth

temperature to 700˚C, graphene flakes were generated on the whole Al_2O_3 substrate (Figure 4-12b). The thickness of these graphene flakes in sample b is in the range of 0.7 ~ 1 nm measured by AFM (Figure 4-12f), which can confirm that monolayer graphene has been synthesized at 700˚C. When further decreasing the temperature into 650˚C, the whole substrate was partly covered with graphene flakes, which indicates the temperature of 650˚C is not able to provide enough energy for the growth (Figure 4-12c). Therefore, on Al_2O_3 substrates, monolayer graphene growth favours a lower temperature of 700˚C, while bilayer or multilayer graphene prefers a higher temperature of 750˚C, which can promote a uniform coverage of the whole substrate, alleviate defects and disorders, and enlarge the crystal size at the same time. More importantly, the morphology of graphene grown on Al_2O_3 at 700˚C has similar layer-by-layer structures as that grown on SiO_2 at 750˚C (Figure 4-12d), while no graphene was grown on SiO_2 substrates at a temperature below 700˚C (Figure 4-12e), as confirmed by Raman spectra of SiO_2 in Figure 4-13a.

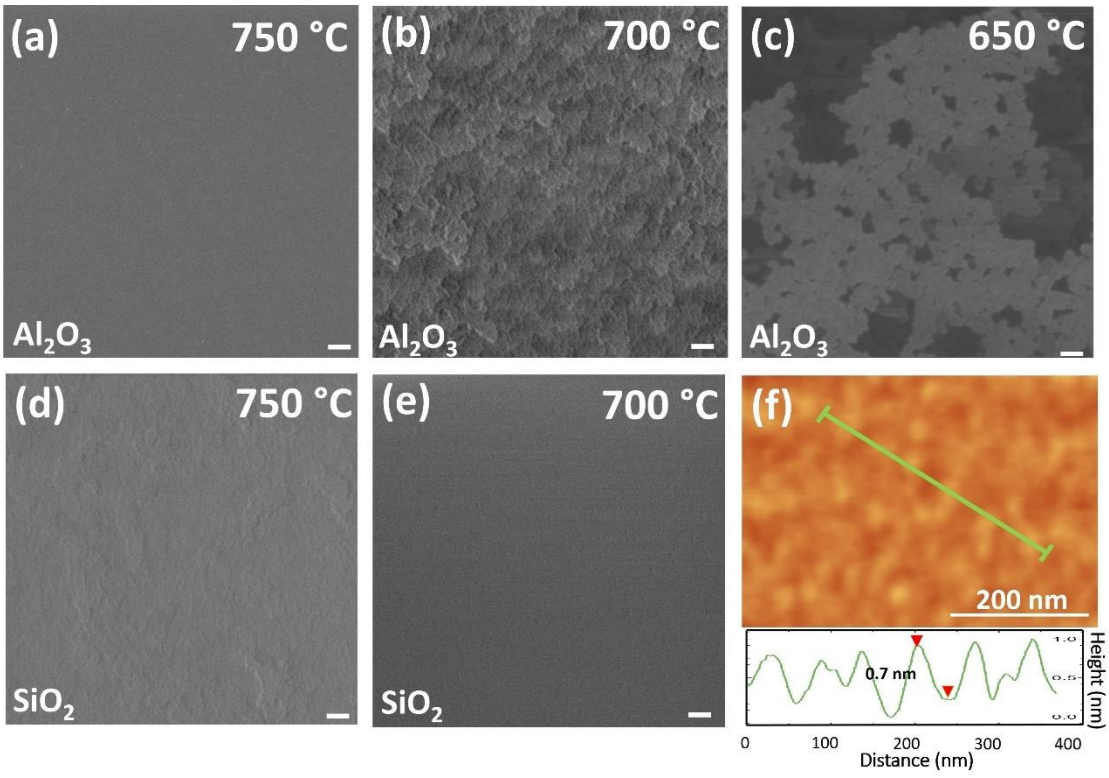

Figure 4-12 Comparison of the growth under different temperatures with 30% NH_3 on Al_2O_3 substrates for 3 hours. SEM images of graphene grown at a temperature range of 750˚C to 650˚C on Al_2O_3 (a-c), and 750°C to 700˚C on SiO_2 (d-e). The scale bars are 200 nm. (f) AFM image of sample (b) and the thickness of its graphene flakes.

It's found that the optimal growth temperature is different for SiO_2 and Al_2O_3, and Al_2O_3 demonstrated its potential as a better substrate for the growth at relatively low temperature. On the SiO_2 substrates, low temperature like 650°C or 700°C is unable to provide enough energy for the growth, however, for Al_2O_3 substrates, graphene can still be synthesized at 700°C with similar structures as the samples grown on SiO_2 at 750°C. Therefore, the growth-temperature windows of these two insulators are different, which implies insulators might have different catalytic effect on the graphene growth.

The corresponding Raman spectra are shown in Figure 4-13a, and the sizes of graphene grown on Al_2O_3 substrates with calculated I_{2D}/I_G are plotted in Figure 4-13b.

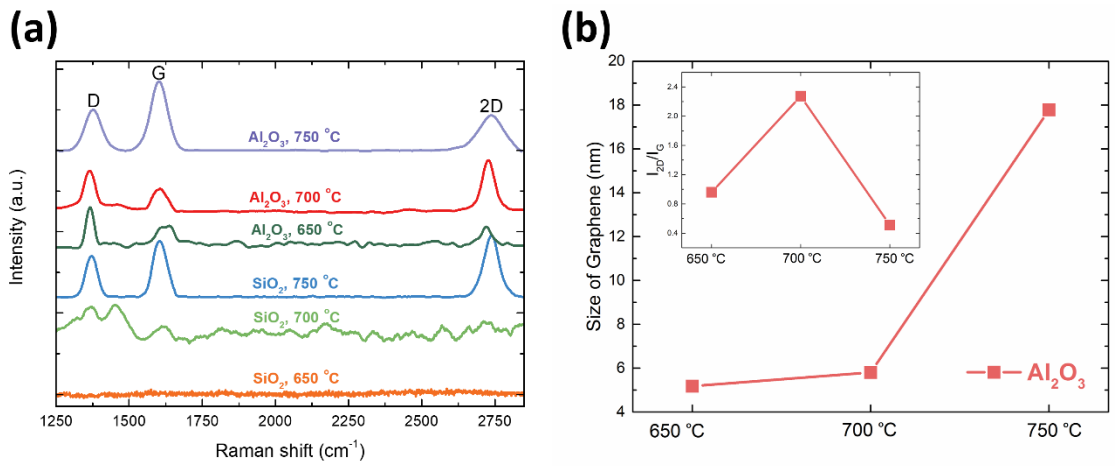

Figure 4-13 (a) Corresponding Raman spectra of graphene samples grown on SiO_2 and Al_2O_3 substrates in the temperature range of 650 ~ 750°C. (b) The temperature dependence of graphene crystalline size and I_{2D}/I_G for graphene films grown on Al_2O_3 substrates.

At 750°C, the Raman spectrum of graphene on Al_2O_3 shows a very board 2D peak with a minimum I_{2D}/I_G of 0.51 and a maximum graphene size of 17.8 nm, implying that bilayer or multilayer graphene has been synthesized. When decreasing the temperature to 700°C, the graphene on Al_2O_3 substrate presents a high density of defects (I_D/I_G ~ 1.8) due to the disorder and asymmetry of graphene caused by a large amount of domain boundaries and defects inside the nanographene. Although the density of defects is high, a sharp 2D peak (I_{2D}/I_G ~ 2.27 with the FWHM of 50.3 cm^{-1}) corresponds to monolayer graphene, which is confirmed with the thickness measured by AFM. By further decreasing the temperature to 650°C, the increased I_D/I_G indicates a very high density of defects and meanwhile the crystal size of graphene is further reduced as Figure 4-13b shows. This temperature dependence analysis suggests the high-temperature can

promote a uniform and better coverage of the whole substrate, alleviate density of defects and enlarge the crystal size at the same time.

Park *et al.* carried out DFT calculations of activation barriers among Cu, Ni, and Al_2O_3 for graphene growth, and their quantitative study demonstrated the catalytic function of Al_2O_3 that enables the graphene growth at low temperature.[229] According to their study, the nucleation and growth of graphene on Al_2O_3 consist of the adsorption and dehydrogenation of the hydrocarbon gas at the catalytically active tricoordinated Al_{III} sites, and the supply and withdrawal of the C adatom during graphene formation, as shown in Figure 4-14. The overall activation energy barrier is the sum of the dissociative adsorption energy of hydrocarbon gas (E_{ad}), surface diffusion barrier for the generated C adatoms (E_d), attachment barrier for additional C adatoms to contact with the anchored C adatom (E_{att}), desorption energy for the C adatom desorbs from the substrate or diffuses across the surface (E_{des}), and the detachment barrier for a C atom from the perimeter of the graphene nucleus (E_{det}). They compared Al_2O_3, Cu, and Ni as the substrate for the graphene growth *via* theoretical calculations. Various surface activation barriers as described above, C solubility, and activation barrier for nucleation were calculated. Among these activation barriers, the supply of C adatoms governed by E_{ad} and the enlargement of the graphene nuclei governed by E_{att} determine the lowest possible growth temperature.[229] From their theoretical calculation, both E_{ad} and E_{att} of Al_2O_3 are much lower than those of Cu while equal to the value of Ni, indicating the growth temperature of graphene on Al_2O_3 should be comparable to that on Ni (nearly the room-temperature growth has been reported). Moreover, Al_2O_3 owns the lowest E_d, which determines the homogeneity of the graphene film, thus implying Al_2O_3 is the most favourable substrates for the homogeneous growth among these three. In conclusion, based on the theoretical calculations, Al_2O_3 shows the great capacity for the low-temperature and homogeneous growth of graphene.

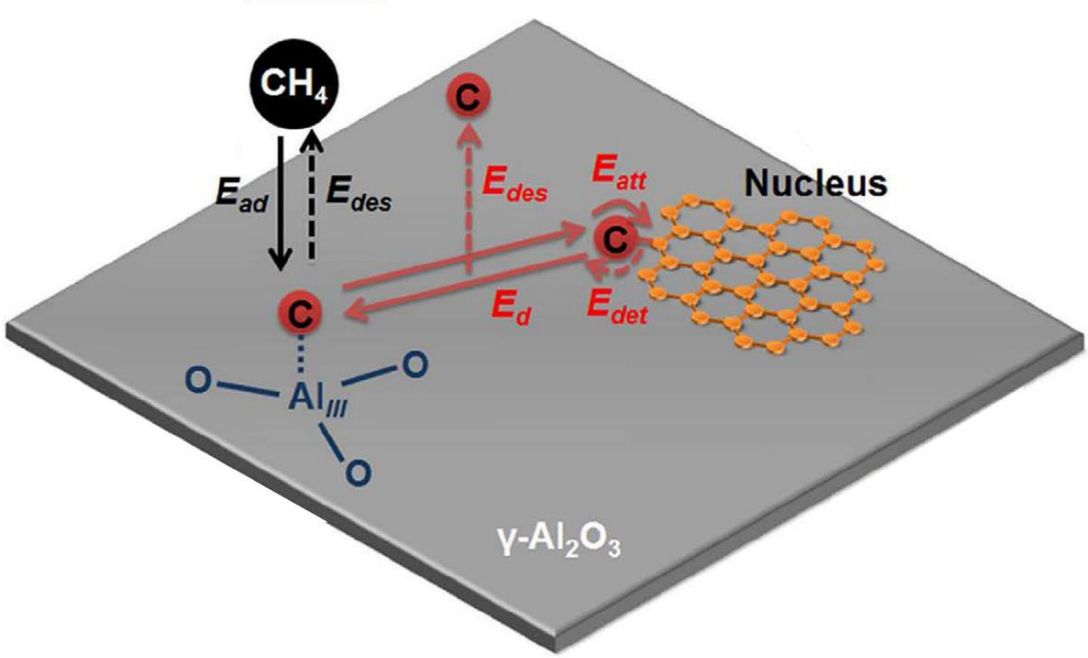

Figure 4-14 Schematic illustration of the nucleation and growth of graphene on γ-Al_2O_3. *Figure from Park et al.*[229]

Besides Al_2O_3 and SiO_2, other insulators including HfO_2, TiO_2, MnO_2, quartz, and sapphire have also been used as substrates under the same condition. As their Raman spectra with low 2D peaks and high D peaks show in Figure 4-15, they are not as suitable as Al_2O_3 to produce monolayer and low-defect graphene at 700°C. Therefore, the similarity and difference in the morphology of graphene on various insulators suggest that insulators might have different growth windows due to their different activation barriers, and these experiments demonstrate that Al_2O_3 substrates have the lowest activation barrier among others, which enables it to produce the similar structures at relatively low temperature. Further theoretical studies *via* DFT simulations to calculate the activation barriers of various insulators are still needed in the future, which will be beneficial to understand the potential of different insulating substrates for the low-temperature growth of graphene.

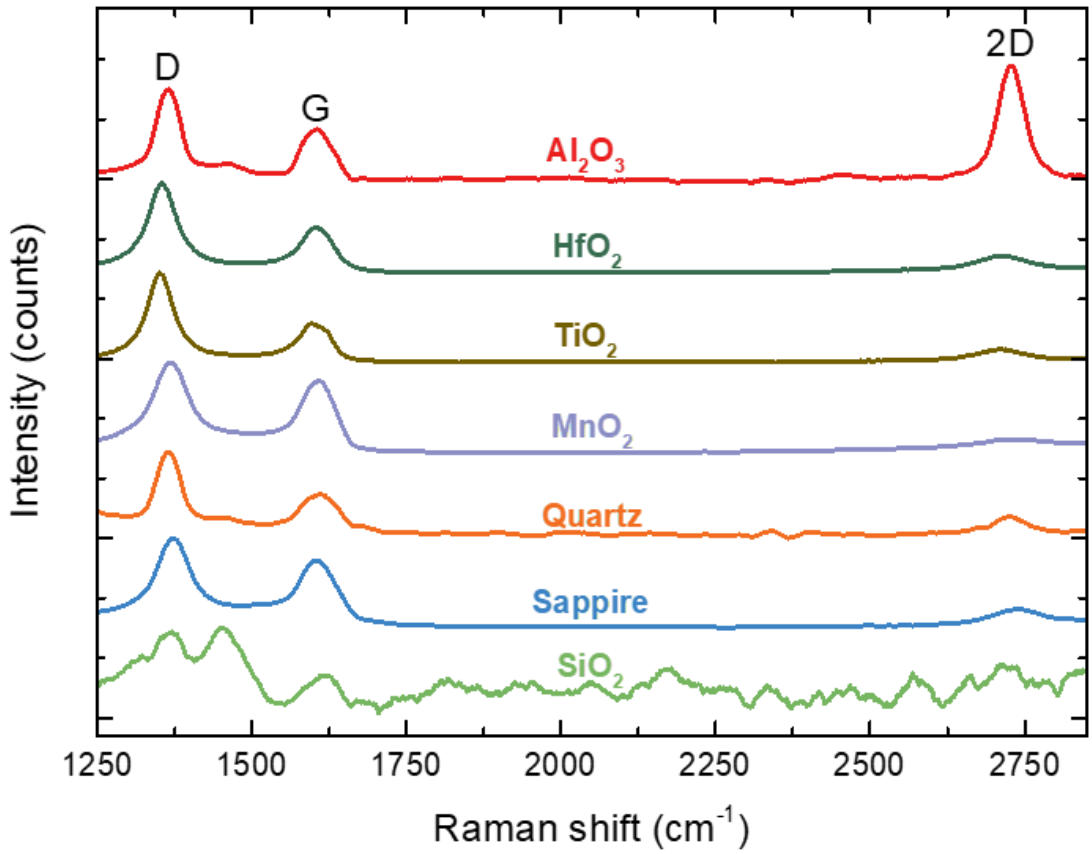

Figure 4-15 Raman spectra of graphene sheets grown on different insulators with 30% NH_3 at 700°C for 3 hours.

4.4 Electrical Characterization

4.4.1 Graphene FETs

To determine the electrical transport behaviour of the synthesized graphene, back-gated graphene FETs were fabricated directly using the as-grown samples without any post-transfer process. By using EBL, oxygen plasma etching, metal deposition (5 nm Cr/50 nm Au), and lift-off technology, numbers of graphene FETs can be fabricated each time other than a single graphene domain device reported in previous work,[89,92,93]. The OM image of a typical graphene FET and its schematic structure are shown as the insets in Figure 4-16c,d. The channel width is 5 μm and the channel length is 2 μm.

Electrical characteristics were measured at room temperature in ambient atmosphere in a Keithley probe station. Figure 4-16a gives the transfer curves ($I_{DS} - V_{BG}$) of five typical graphene FETs fabricated from the sample of graphene prepared under 30% NH_3 (Figure 4-7j). For comparison, the transfer curve of a FET prepared under only H_2 and C_2H_2 is plotted in Figure 4-16b. The total gas flow, the C_2H_2 concentration, the growth time and temperature, and the device fabrication steps for the

two groups of samples were the same. Figure 4-16c,d shows the corresponding output curves (I_{DS} − V_{DS}) at various gate voltages (from −40 V to 40 V with a step of 20 V). The symmetrical linear behaviour implies an ohmic contact between electrodes and graphene channel has been formed. The FETs of graphene grown under 30% NH_3 show an ambipolar transfer characteristic with the Dirac point at negative gate voltages (−20 ~ −30 V), indicating a typical n-type behaviour. The shift value of the Dirac point is consistent with previous reports using ammonia in the growth.[89,228] However, the FETs fabricated from graphene samples grown under C_2H_2/H_2 plasma does not exhibit such an ambipolar transfer characteristic yet even though the gate voltage spans from −60 ~ +60V. Other groups also observed the similar p-doped behaviour of the graphene grown in only H_2 as an etching gas.[77] The reasons for that can be: (1) the strong doping of the substrates;[63] (2) the doping effect from the metal (Cr/Au), which has been proved experimentally and theoretically.[230,231] After introducing NH_3, the Dirac point position moved from positive V_{BG} to negative V_{BG} implying the transition of graphene from p-type to n-type. Since NH_3 was the only variable in this control experiment, this indicates that the introduction of NH_3 has an n-type doping effect on the as-grown graphene, while the graphene is normally p-type FET behaviour without NH_3.

The mobility values for the n-doped graphene FETs were extracted from the slope of I_{DS} – V_{BG} using the equation $\mu_{FET} = \frac{dI_{DS}}{dV_{BG}} \times \frac{L}{WC_{ox}V_{DS}}$, where dI_{DS}/dV_{BG} is the slope of the transfer characteristic of the device at $V_{DS} = 100$ mV, L and W are the channel length and width. C_{ox} is the back-gate capacitance per unit area between the channel and the back-gate and can be calculated to be 115 aF/μm^{-2} by $C_{ox} = \varepsilon_r \varepsilon_0 / t_{ox}$, where ε_0 is the permittivity of free space, ε_r is the relative permittivity of silicon dioxide and t_{ox} is the oxide thickness. The average field-effect mobility was estimated to be 14 ~ 16 cm^2/Vs.

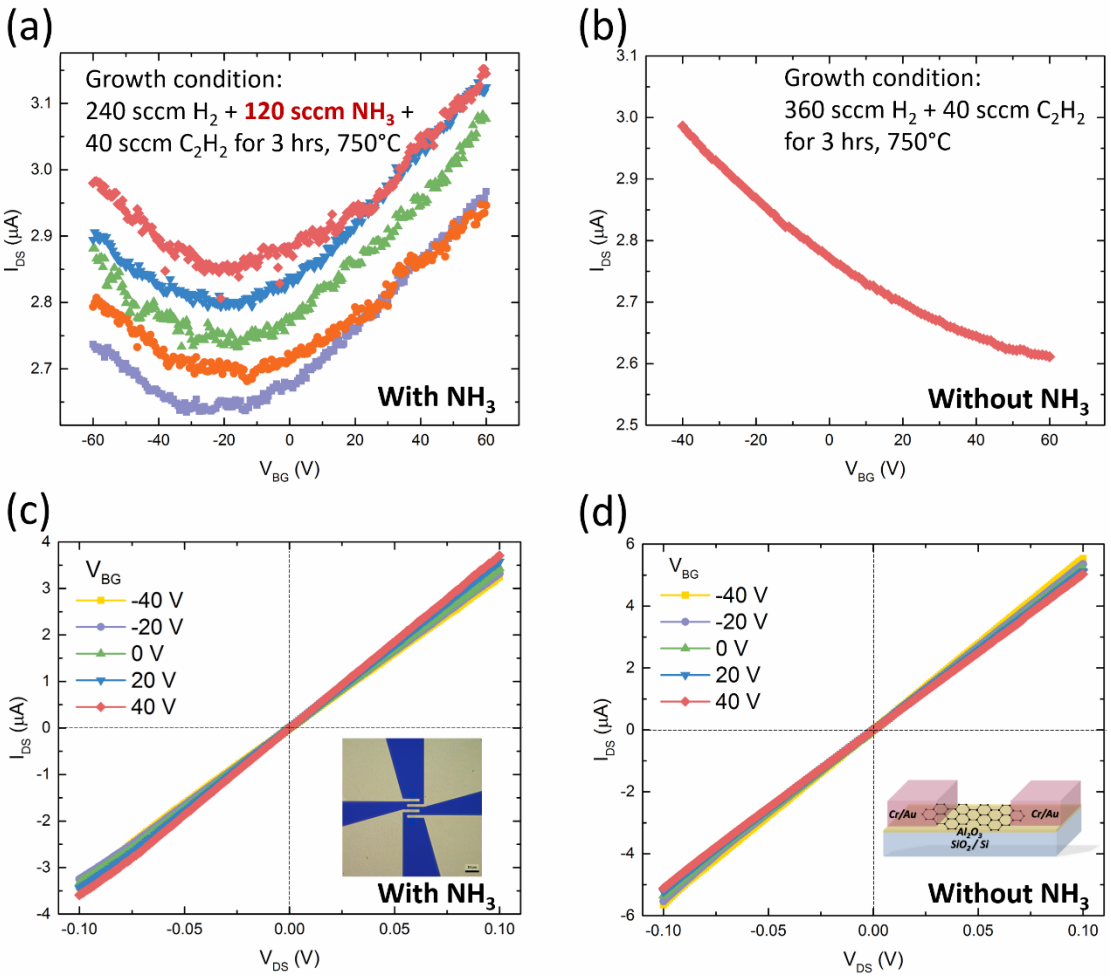

Figure 4-16 Transfer curves of (a) 5 typical FETs of N-doped graphene synthesized with NH_3 and (b) a typical FET of pristine graphene synthesized in only H_2 and C_2H_2 ambiance (V_{DS} at 100 mV). (c-d) The corresponding output curves at different gate voltages and the inset is the schematic image of the device, and the OM image of the graphene device (the scale bar is 10 μm).

4.4.2 Sheet Resistance

The four-point probe is a commonly used method to measure the sheet resistance. Figure 4-17 is a schematic of four-point probe configuration where the four probes are set collinearly at equal interval *S*. In general, for probe spacings S_1, S_2, and S_3, the voltage at probe 2 is

$$V_2 = \frac{I\rho}{2\pi}\left(\frac{1}{S_1} - \frac{1}{S_2 + S_3}\right) \tag{4-3}$$

and at probe 3 it is

$$V_3 = \frac{I\rho}{2\pi}\left(\frac{1}{S_1+S_2}-\frac{1}{S_3}\right) \tag{4-4}$$

the total measured voltage $V = V_{23} = V_2 - V_3$ becomes

$$V = \frac{I\rho}{2\pi}\left(\frac{1}{S_1}-\frac{1}{S_2+S_3}-\frac{1}{S_1+S_2}+\frac{1}{S_3}\right) \tag{4-5}$$

for the four-point probe setting used in this study, the probe spacings are equal. With $S = S_1 = S_2 = S_3$, the surface resistivity can be expressed as

$$\rho = 2\pi S\frac{V}{I} \tag{4-6}$$

in the case of thin samples, the sheet resistance can be calculated by[175]

$$R_{sh} = \frac{\rho}{t} = \frac{\pi}{\ln(2)}\frac{V}{I} = 4.532\frac{V}{I} \tag{4-7}$$

Figure 4-17b shows a typical four-point probe measurement of the voltage potentials at probe 2 and probe 3. The sheet resistance of the graphene grown on Al_2O_3 is calculated to be 13.6 kΩ/□, while for the use of SiO_2 substrates, the sheet resistance is 24 kΩ/□.

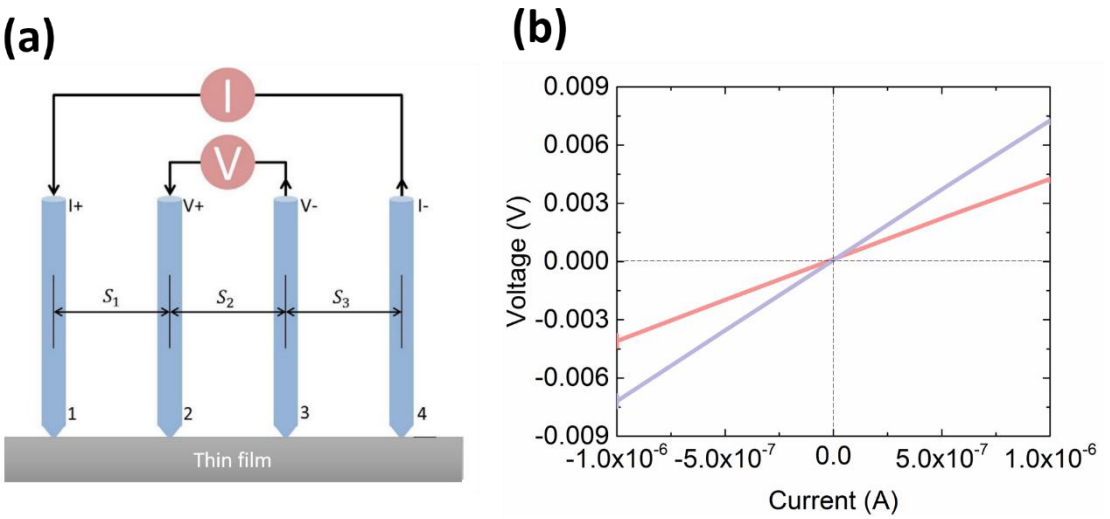

Figure 4-17 (a) Schematic illustration of four-point probes with current flow and voltage measurement. (b) I-V curve of a typical sample under probe arrangements.

Table 4-1 shows a summary of the recently-reported PECVD methods to synthesize graphene on insulating substrates. Various aspects are compared including sheet resistance, field-effect mobility, growth temperature, and quality of the film. From the previous papers, two challenging issues facing the direct growth of graphene by PECVD are (1) nanographene, 3D structures or linear defects that result in very high D

peak and (2) discontinuous single graphene domains that limit its further applications for large-scale fabrications. By introducing NH_3 into the growth, the graphene film synthesized in this work owns the lowest D peak among all the PECVD results, and the continuous film without any 3D structures or linear defects enable it for numerous devices fabricated on the same chip other than just a single graphene domain device.

Table 4-1 Summary of electrical properties and film quality of graphene synthesized on insulators by PECVD method.

No	Reference	R_{sheet} kΩ/□	Mobility cm^2/Vs	Temperature ˚C	Quality
1	Sun, J. et al.[95]	N/A	N/A	800-900	Very high D peak, 3D structures
2	Chugh, S. et al.[94]	1.3	N/A	650	Very high D peak, 3D structures
3	Kim, Y. S. et al.[96]	1.4	105	500-900	Single graphene domain device
4	Muñoz, R. et al.[88]	3.4	NA	650-700	Single graphene domain, linear defects
5	Wei, D. et al.[89]	4.1	100-400	650	Single graphene domain device
6	This work	13.6	14-16	700-750	Lowest D peak, continuous graphene
7	Medina, H. et al.[98]	20	N/A	400	Very high D peak, transfer needed
8	Yang, W. et al.[99]	20	15	550	High D peaks, nanographene
9	Liu, D. et al.[93]	32.7	70	510-545	Single graphene domain device
10	Zhang, L. et al.[91]	40	N/A	550	High D peak, 3D structures

4.5 Discussion

Why can the growth mode of graphene be changed from 3D nano-walls to layer-to-layer films, and why is it n-type doped? Previous studies have shown that NH_3 is a much stronger etchant than H_2 to produce atomic hydrogen under plasma conditions, which can selectively etch away the amorphous carbon on graphene and remove defects generated at the graphene edges, thus keeping the edges atomically smooth and active during the graphene crystal growth.[89,220,228] The whole chemical reaction is a balance between the graphene nucleation/growth by C_2H_2 and the removal of excess carbon by atomic hydrogen. The reactions of graphene formation by C_2H_2 plasma and etching process by NH_3 and H_2 plasma can be expressed by the following reversible equilibriums:[92,232]

$$\begin{gathered} C_2H_2 \rightleftharpoons C_xH_y + H\cdot \rightleftharpoons \text{graphene} + H_2 - Q \\ NH_3 \rightleftharpoons N_mH_n + H\cdot \rightleftharpoons N_2 + H_2 - Q \\ H_2 \rightleftharpoons H\cdot \end{gathered} \tag{4-8}$$

where Q is heat. In the plasma state, C_2H_2 is dissociated into C_xH_y radicals and atomic hydrogen, while both NH_3 and H_2 are the generators of atomic hydrogen. When there is no NH_3 or the NH_3 concentration is low, the atomic hydrogen is insufficient to suppress the decomposition of C_2H_2, leading to a high level of carbon generation. The unnecessary carbon will create double nucleation and form 3D vertically erected graphene walls on the substrates. By increasing the NH_3 concentration, the decomposition of NH_3 is the dominant reaction over the decomposition of C_2H_2 due to its weak bonds.[34] The sufficient hydrogen generated by NH_3 together with the introduced hydrogen will decelerate and weaken the decomposition process of C_2H_2, generating a controlled amount of carbon necessary for the growth of graphene and resulting in layer-by-layer graphene flakes to form continuous films. Consequently, the amount of NH_3 plays a critical role in the growth of graphene owing to the generated atomic hydrogen balancing the production of reactive hydrocarbon radicals and the removal of amorphous carbon during the PECVD process.

However, this could not well answer the questions. In fact, the reactions in the plasma is very complicated, which can hardly be explained by a few simple chemical reaction equations. It depends not only on the plasma type (for example, DC plasma, RF inductively coupled plasma (ICP), microwave plasma etc.) and the plasma power, but also on the plasma gases and pressure. Mao *et al.* intensively investigated the plasma chemistry of different binary gas mixtures (CH_4/H_2, CH_4/NH_3, C_2H_2/H_2 and C_2H_2/NH_3)

for the synthesis of CNTs/nanofibers by ICP enhanced CVD.[233] It is found that tens of species will be formed in the plasma. Although the atomic hydrogen produced by CH_4/NH_3 plasma is significantly higher than that by CH_4/H_2 plasma at 1 Torr or high pressure, the atomic hydrogen produced by C_2H_2/NH_3 plasma is similar to that by C_2H_2/H_2 plasma. The most fundamental thing is that long-chain hydrocarbons such as $C_{2n}H_2$ and $C_{2n}H_6$ (n up to 6) are formed and become important in the C_2H_2/H_2 plasma. On the contrary, the formation of these long-chain hydrocarbon is less important in the C_2H_2/NH_3 plasma. Some long-chain hydrocarbons under C_2H_2/H_2 plasma can deposit randomly onto the substrate and develop into 3D nano-walls. By introducing higher concentration of NH_3 the formation of long chain hydrocarbon is greatly suppressed, therefore the growth of 3D nano-walls is eliminated. Moreover, the atomic hydrogen is believed to play an important role in the system. This is because NH_3 can be thermally decomposed enough atomic hydrogen on the surface of substrate at 650 ~ 750°C.[234] while the thermal decomposition of H_2 can be ignored due to its high stability. This explains why the quality of graphene is improved by introducing NH_3.

On the other hand, active HCN species can be also produced in the plasma, which can attach to the edge of graphene and form the substitutionally N-doped graphene. The free $-C=C-$ and $-C=N-$ groups are likely the intermediates, and should couple with each other going through further dehydrogenation and forming small domains of sp^2 hybridized carbon containing N and then grow into N-doped graphene film as shown in Figure 4-18. This results in amounts of graphitic N,[228] leading to a Dirac point shift at a negative gate voltage and the downshifts of the G peaks in Raman spectra. As discussed earlier, a Dirac point shift to negative gate voltages (−20 ~ −30 V) has been observed in the transfer characterization of the FETs using the graphene synthesized with the assist of NH_3. The n-type doping of graphene can be also confirmed by Raman spectroscopy. The Raman spectra in Figure 4-8a,b show large downshifts of the G peaks for samples prepared under different NH_3 concentrations (11.8 ~ 13.5 cm^{-1} for SiO_2 samples and 16.7 ~ 21.6 cm^{-1} for Al_2O_3 samples) compared with the sample without using NH_3. This is in accordance with reported N-doped graphene,[89,235] but different from Ref.[236] Study has demonstrated that substitution of C atoms with graphitic N is n-type doping with a downshift in G peak, while pyridinic and pyrrolic N is p-type doping with a upshift in G peak.[237] This means that the as-grown graphene is substitutionally doped by nitrogen atoms.

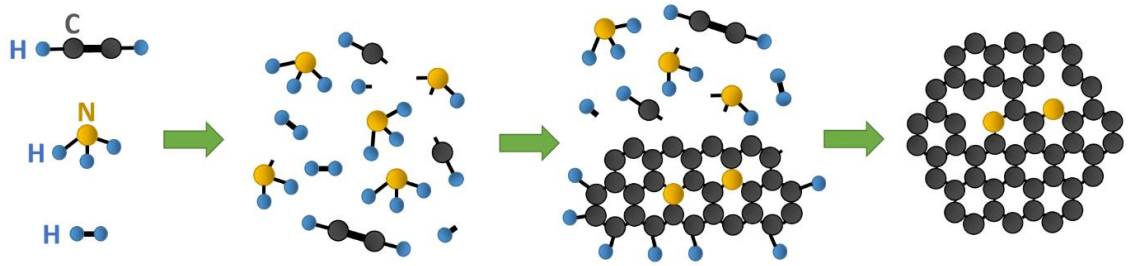

Figure 4-18 Scheme of a proposed mechanism for the synthesis of N-doped graphene *via* the reaction of C_2H_2, H_2, and NH_3, where grey balls represent C atoms, blue for H, and yellow for N.

4.6 Summary

In summary, a microwave PECVD method of graphene synthesis on both SiO_2 and Al_2O_3 substrates without using any metal catalysts has been investigated. The effect of different carbon sources on the synthesis has been compared. By introducing NH_3 to suppress the formation of long-chain hydrocarbon in the plasma and to enhance the etching effect, uniform and continuous graphene films with the lowest density of defects among all the PECVD growth of graphene can be obtained. Further investigation of the effect of insulating substrates on the growth shows that the growth-temperature window and catalytic effect are different for each insulator owing to the different activation barrier. Al_2O_3 seems to own a lower activation barrier, which makes it a promising candidate as the substrate for the metal-catalyst-free growth of graphene at low temperature. This direct assembly of graphene on high-κ Al_2O_3 thin films can be flexibly incorporated into electronic and optoelectronic devices without any post-growth transfer process. More improvements are still needed in largely increasing the grain size, further reducing the growth temperature, and better controlling the number of layers. This work provides an important step towards large-scale, low-cost, and high-quality synthesis of graphene on arbitrary substrates.

5 GRAPHENE AND WS_2 HETEROSTRUCTURE FIELD-EFFECT TRANSISTORS

In this chapter, an effective approach of reducing the contact resistance in WS_2 field-effect transistors (FETs) based on the metal/graphene hetero-contacts has been demonstrated. By inserting monolayer graphene between the metal and WS_2 interface, the Fermi level pinning at the metal and WS_2 interface can be eliminated and the Schottky barrier heights can be significantly reduced. Both high work function and low work function metals have been investigated in the metal/graphene contact to WS_2. By shifting the Fermi level of graphene with metal contacts and changing the gate voltage, the contact resistance can be further reduced. As compared to the conventional metal-WS_2 contacts, the on-current values can be increased by 2 ~ 3 orders of magnitude with a graphene insertion layer, and the lowest contact resistance has been obtained in Au/Cr-graphene-WS_2 FETs with on/off ratio of 10^6 and mobility up to 51.6 cm^2/Vs at room temperature.

5.1 Introduction

Transition metal dichalcogenides (TMDs) have attracted significate attention as promising atomically thin semiconductors. Unlike graphene without a bandgap that limits its further use in field-effect transistors (FETs), TMDs are semiconductors with a finite bandgap while retain atomically thin 2D structures and reasonably high mobilities.[104,238] The layered TMDs with a few-atom thickness have been regarded as ideal channel materials in ultrathin short channel devices, and have exhibited a significant potential to solve the device scalability issue that the current silicon technologies have encountered. With the van der Waals interaction, TMDs can be flexibly integrated with different materials without the limitation of lattice matching, which opens up the possibility of next-generation functional electronic and optoelectronic devices, such as atomically-thin-body FETs, tunable photovoltaic devices, light emitting devices and gas sensors.[238,239]

However, the large contact resistance at the interface between any bulk metals and 2D TMDs drastically restrains the drain currents and degrades the transport properties of FETs.[6,240] The main reason is the strong Fermi level pinning exists at the interface of metal and TMDs, resulting in the shift of Fermi level towards E_{CNL}. As one of the TMD materials, WS_2 has recently become a focus of study due to its indirect-to-direct band-gap tunability, giant spin splitting, and valley-related physics.[241] Nevertheless, the E_{CNL} of WS_2 is located at the mid-gap with a large Schottky barrier height, which makes it even more challenging to obtain a low contact resistance.[116,242] The degradation in transport properties is usually observed in WS_2 FETs, and the device performance is mainly restricted by the large contact resistance at the metal/WS_2 junction.[6]

Two traditional methods have been commonly used to reduce the contact resistance. One is doping technique, which has been proved to create an ohmic-like Schottky barrier by heavily doping TMDs by molecules or ions (PEI,[165] benzyl viologen molecular doping,[166] chloride molecular[167] and lithium fluoride,[168]) or gas driven doping under deep ultraviolet light[169] and high-pressure annealing.[170] However, the air instability of chemical doping is a critical issue to form highly stable and reliable contacts because the absorbed chemical species may detach from the surface or react with oxygen and water from surroundings in the long-term exposure in ambient air.[171] Another approach is to use metal electrodes with a work function close to the conduction band or valence band of the TMD materials.[112] Ultralow work function metal like scandium has been used to form an Ohmic contact to MoS_2, with enhanced

electron injection and lower contact resistances.[112] However, low work function metals are highly reactive to be oxidized or fast diffusing to other layers thus affecting the device performance.[243] In the case of WS_2, both DFT calculation[111] and experimental work[116] have demonstrated a strong Fermi level pinning exists near the mid-gap of WS_2, which results in a significantly large Schottky barrier height unable to be effectively modulated by simply changing the metal materials.

Early study of using CVD or exfoliated graphene as reliable S/D electrodes and gate contacts to TMDs has attracted great attention.[139] This all 2D material FET provides a unique device architecture for future applications and offers a novel approach to improve the poor conventional metal contact to TMDs. The graphene-TMD contact to release the Fermi level pinning and lower the contact resistance has been further studied and applied to MoS_2,[139,142,143,145,147,148] WSe_2,[140] and WS_2.[138,150,163,244] Recent study using probe force microscopy to examine the graphene/WS_2 junctions has demonstrated the great potential of graphene to form an low-resistance contact to WS_2.[245] Nevertheless the mechanism of different metal/graphene hetero-contacts to WS_2 has never been explored yet, and the shift of graphene Fermi level to WS_2, especially with different metals, still remains unclear.

In this study, the metal-WS_2 contact and metal-graphene-WS_2 contact in WS_2 FETs using a high work function metal (nickel) and a low work function metal (chromium) have been investigated, respectively. A strong Fermi level pinning to the conduction band has been observed in the WS_2 FETs with four conventional metal contacts of Ti, Cr, Ni and Pd, which is consistent with previous works. By introducing monolayer graphene between the metal and WS_2, devices exhibit p-type behaviour, indicating the Fermi level pinning effect has been eliminated. The shift of the Fermi level to the valence band can be controlled by choosing the metal contact to graphene and changing the gate voltage, leading to the increase of the hole current and making p-type WS_2 FETs possible. Owing to the graphene insertion layer, the on-current can be significantly increased by 2 ~ 3 orders of magnitude higher for metal-G-WS_2 contacts with the lowest contact resistance of 0.0225 kΩ·μm achieved in Au/Cr-graphene (G)-WS_2 FETs.

5.2 Experimental Methods

5.2.1 Synthesis of Monolayer Graphene

Large-area and high-quality monolayer CVD graphene was synthesized on copper foil by CVD at atmospheric pressure. First, copper foil (Alfa Aesar, 99.8% purity, 25 μm thickness) was electropolished and then rinsed by IPA and DI water. After loading the copper foil into a 2-inch quartz tube furnace, the system was heated up to 1030°C in argon ambiance and then the copper foil was annealed for 5 min. Graphene growth was carried out by introducing hydrogen and methane for 80 min, followed by cooling down to room temperature under the same argon and hydrogen flow (without methane). Details of the graphene synthesis have been described in my group's previous paper.[246]

5.2.2 Transfer of WS_2 and Graphene

High-quality WS_2 flakes were first mechanically exfoliated from a bulk WS_2 crystal (purchased from 2D Semiconductors, Inc.) with scotch tape, subsequently transferred from scotch tape onto a PDMS stamp, and finally the PDMS supported WS_2 flakes were transferred onto a heavily p-doped Si substrate with 300 nm SiO_2 capping layer. This transfer method can avoid the residues and contamination from the scotch tape and obtained thin WS_2 flakes large enough for the following device fabrication. The as-grown monolayer CVD graphene was separated from Cu using the graphene transfer method.[246] The graphene/Cu sample was first spin-coated with a PMMA layer at 5000 rpm for 40 seconds and dried at room temperature. Graphene film on the backside of the copper was removed using oxygen plasma etching, and the copper foil was etched away using 0.05M ammonium persulfate solution. The floating PMMA/graphene film was transferred to DI water three times with at least 30 min per rinse, and then transferred onto the WS_2/SiO_2 substrate and dried at room temperature. Finally, PMMA was dissolved by acetone, and the graphene/WS_2/SiO_2 sample was rinsed in IPA and dried with N_2. Before device fabrication, the sample was baked at 160°C for 3 hours to improve graphene adhesion on the SiO_2 substrate.

5.2.3 Device Fabrication

Figure 5-1a depicts a schematic of a back-gated WS_2 FET with monolayer graphene as an insertion layer between metal and WS_2, while Figure 5-1b shows a conventional back-gated WS_2 FET with direct metal contacts as S/D electrodes. Figure 5-1c,d,e are

the OM images of important device fabrication steps. Briefly, after the transfer of Cu-catalysed CVD graphene, mechanically exfoliated WS_2 flakes were transferred onto SiO_2 (300 nm)/p-Si substrates as shown in Figure 5-1c. EBL was used to pattern the area of graphene, followed by low power oxygen plasma RIE to isolate the S/D and the different devices (Figure 5-1d). The graphene above the channel was fully etched. The channel length is kept at ≈ 2 μm and the channel width varies in the range of 1 ~ 3 μm depending on the size and shape of the transferred WS_2. The pattern for metal S/D above graphene were defined by EBL, with the size 100 nm smaller at each side than graphene contacts as illustrated in Figure 5-1a. Metal electrodes (50 nm Ti, Ni and Pd, 5 nm Cr/45 nm Au) were deposited on the top of graphene contacts separately, forming the metal/graphene/WS_2 junctions (Figure 5-1e). Hence, this device (metal-graphene (G)-WS_2 FETs) has WS_2 as the channel, SiO_2 (300nm)/Si substrate as the back-gate, and graphene/metal as S/D electrodes. In order to investigate the effect of graphene insertion layer on the device, WS_2 FETs with direct metal S/D contacts (metal-WS_2 FETs) were fabricated as control devices using the same fabrication procedure and WS_2 flakes of a similar thickness.

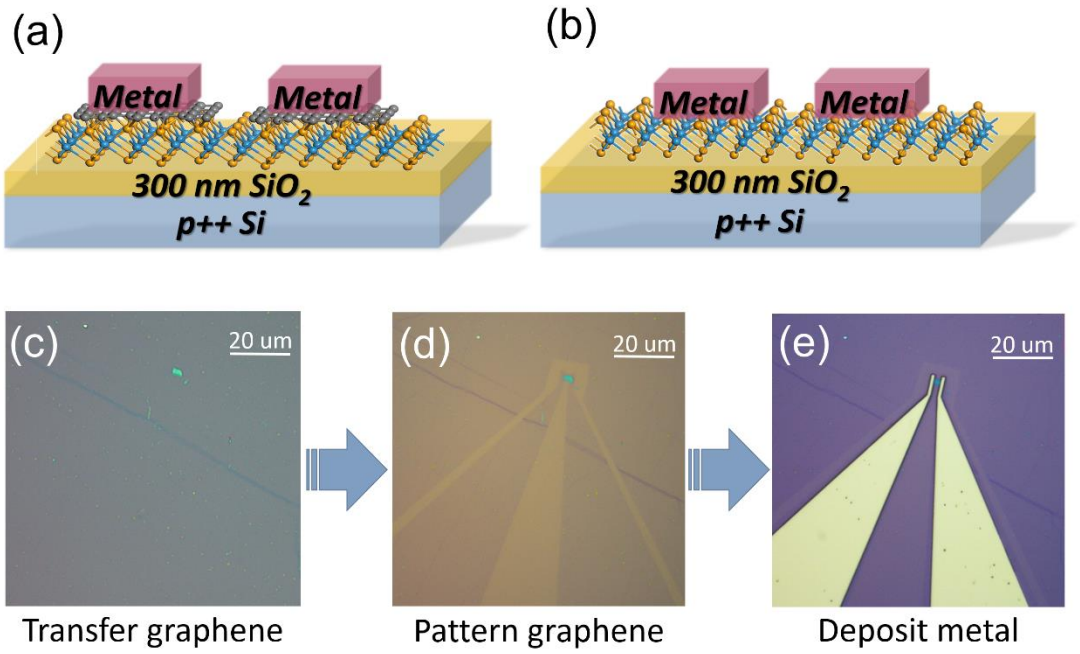

Figure 5-1 Schematic of back-gated WS_2 FETs with (a) monolayer graphene as an insertion layer and (b) direct metal and WS_2 contacts. OM images of important fabrication steps including (c) transfer CVD monolayer graphene onto the WS_2/SiO_2 sample, (d) pattern graphene using EBL, and (e) deposit metal electrodes on the top of graphene.

5.3 Material Characterization

5.3.1 Microscopic Techniques

OM, SEM, and AFM are used for the surface characterization of WS_2 and graphene stacks after etching graphene to the shape of the electrodes. Figure 5-2a is the OM image of a typical WS_2 and graphene heterostructure and the dash line areas are the graphene layer patterned as electrodes. The graphene outside the dash line areas were etched away to isolate the devices from each other. Note that the graphene above the WS_2 channel needs to be fully etched so that the device can function normally. The optical contrast difference between 2D materials and substrates in the OM can determine the thickness of 2D materials,[247] and to be more specific, the brighter colour of the 2D flakes indicates thicker layers. Thus, it can be used to confirm the WS_2 and graphene heterostructure has been successfully formed as the colour of the graphene contact areas is brighter than the rest of WS_2. Figure 5-2b shows the SEM image of a WS_2 and graphene heterostructure after O_2 plasma etching. The extra graphene was fully etched away especially the graphene above the channel. To further zoom in the image, the area of the graphene S/D contacts to WS_2 was characterized by AFM (Figure 5-2c). The thickness of graphene is measured to be around 1 nm, so the transferred graphene is confirmed to be monolayer graphene.

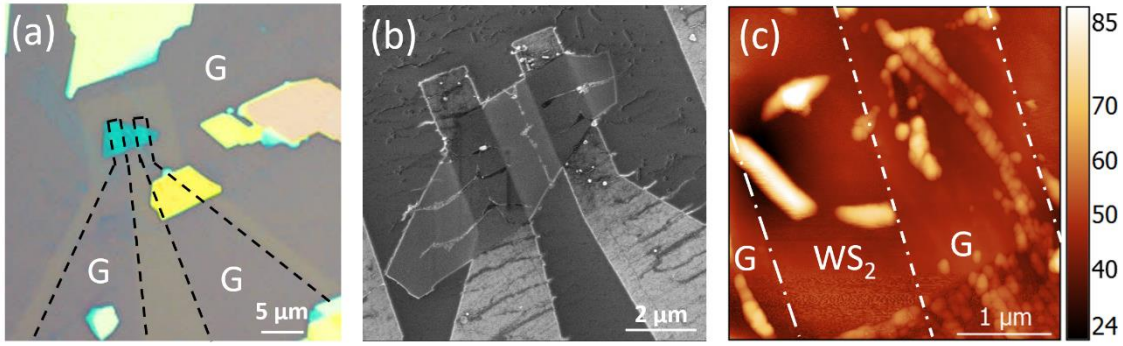

Figure 5-2 (a) OM image of a sample with graphene patterned to the shape of electrodes. (b) SEM image of a graphene and WS_2 stack after graphene being etched away by O_2 plasma. (c) AFM image of the sample in (a). The scale bars are shown inside each image.

5.3.2 Raman Spectroscopy

Raman spectroscopy is used for the characterization of WS_2 and graphene heterojunctions with 532 nm laser excitations, and the spectrum is shown separately in two regions, 280 $cm^{-1} \leq \omega \leq 440$ cm^{-1} and 1200 $cm^{-1} \leq \omega \leq 3000$ cm^{-1}, in Figure 5-3. As

the multi-peak Lorentzian fitting curves shown in Figure 5-3a, the two optical phonon modes (in-plane phonon mode $E^1_{2g}(\Gamma)$ and out-of-plane phonon mode $A_{1g}(\Gamma)$) at the Brillouin zone centre and the second-order longitudinal acoustic phonon mode $2LA(M)$ at the M point are the most prominent feature of WS_2.[191] In the transferred WS_2, the fitted peaks $E^1_{2g}(\Gamma)$, $A_{1g}(\Gamma)$ and $2LA(M)$ are positioned at 353.2 cm^{-1}, 421.5 cm^{-1}, and 357.2 cm^{-1} respectively, which can be used to determine the thickness of WS_2 flakes.[150,177,191] As the thickness increases, the intensity ratio of $2LA(M)/A_{1g}(\Gamma)$ decreases, and the small intensity difference of $E^1_{2g}(\Gamma)$ and $A_{1g}(\Gamma)$ (68.3 cm^{-1}) indicates the triple layer nature of the transferred WS_2.[191,248] The Raman spectrum of graphene is shown in Figure 5-3b after the baseline subtraction. A sharp and symmetric 2D peak with negligible D peak and a I_{2D}/I_G intensity ratio of around 2.7, indicates high-quality, low-defect graphene has been synthesized by Cu-catalysed CVD.[249] As it was reported elsewhere before, these films are monolayer graphene.[246] The Raman spectrum of the WS_2 and graphene heterostructure is the sum of the individual spectrum of isolated WS_2 and graphene, which is in consistence with previous work.[248] This can confirm the van der Waals interface of WS_2 and graphene has been formed.

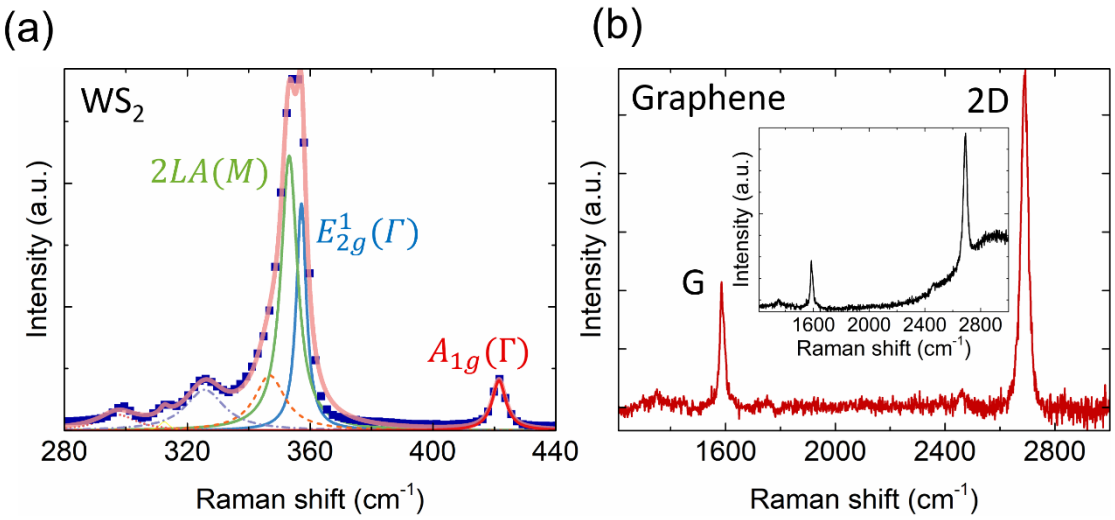

Figure 5-3 Raman spectra of the WS_2-graphene stack. (a) A multi-Lorentzian curve fitting for the Raman spectrum shows signature peaks of WS_2 including the atomic displacements for the in-plane phonon mode $E^1_{2g}(\Gamma)$ (blue), out-of-plane phonon mode $A_{1g}(\Gamma)$ (red), and the second-order longitudinal acoustic phonon mode $2LA(M)$ (green). (b) Raman spectrum of the graphene insertion layer. The inset is the spectrum before the baseline subtraction.

5.4 Optimization of Device Fabrication

5.4.1 Selection of EBL Resist

Two common resists, UV1116-0.5 photoresist (Dow Chemical Company) and PMMA 950 A8 (MicroChem), have been tested in the fabrication of the WS_2/graphene heterostructure FETs. UV1116 is a high-temperature, positive DUV consolidation photoresist with a good process window, and it is generally used in photolithography.[250] Low dose required results in short write-time thus making UV1116 very suitable for relatively large resolution features. UV1116 was primarily used in the WS_2/graphene FETs as it worked well in the graphene FETs as described in Chapter 4. However, it failed as shown in Figure 5-4a, and a large area of graphene film has been damaged in the graphene pattern areas after developing the resist UV1116.

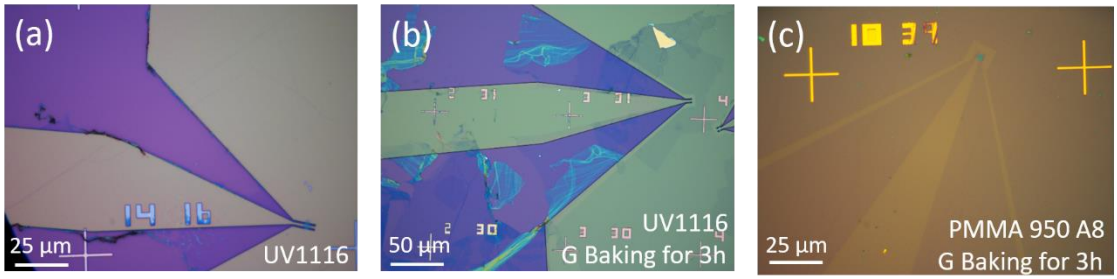

Figure 5-4 OM images of a sample after EBL graphene pattern and resist developing, using (a) UV1116 resist and (b) UV1116 with graphene baked for 3 hours before EBL. (c) Result of PMMA 950 A8 with 3-hour baking for graphene.

The reason might be the transferred graphene did not stick well to the substrate while in the case of the graphene FETs, the graphene was directly synthesized on the substrate, and the 700 ~ 750°C and 3-hour growth enables graphene to have a good adhesion with the substrate. Based on this idea, the transferred graphene samples were baked for 3 hours at 160°C before all the fabrication steps. The situation has been improved as the damage area of graphene was reduced as shown in Figure 5-4b. Then the resist has been changed to PMMA, which is the most popular polymer-based positive resist for EBL, offering high resolution down to tens of nanometres. PMMA has been proved to prevent graphene from damages and Figure 5-4c shows the well-patterned graphene contacts after O_2 plasma etching and PMMA removal. This is probably because UV1116 is quite hard resist, and when it peels off, it would remove graphene underneath, however, PMMA 950 A8 is less hard and the adhesive force

between PMMA and graphene is relatively small, thus it can gently peel off. Therefore, the optimized steps with 3-hour baking treatment and PMMA 950 A8 as EBL resist have been adopted in the following device fabrication procedure.

5.4.2 Adjustment of RIE Time

RIE is very important in the device fabrication, as it isolates the devices from each other by etching away graphene around the device otherwise it will short. Moreover, it etches away the graphene above the WS_2 channel and defines graphene electrodes as S/D contacts. The O_2 plasma RIE time needs to be moderately adjusted, since a longer-time treatment can directly reduce the layer thickness as well as modify the band structure and doping effect thus leading to the change of the electronic properties of TMDs.[251] However, too short RIE time results in the unremoved graphene above the channel. As shown in Figure 5-5, the Ti-G-WS_2 FET with 7-second RIE time displays a typical 'Valley FET' behaviour. The two branches of transfer characteristics dominated by electrons or holes are separated by the Dirac point and the output characteristics show a linear shape without any saturation as most graphene FETs would have, and the FET could not be fully turned off.[252] This unique electrical property indicates the graphene film above the WS_2 channel area was not completely etched away. As a result, this Ti-G-WS_2 FET exhibits a graphene FET-like behaviour mainly due to the graphene-WS_2 combined channel. By increasing the RIE time to 10 s, it is enough and effective to remove the graphene above the channel while without thinning the thickness of WS_2. So, for following devices, the time of O_2 plasma etching is optimized to be 10 s.

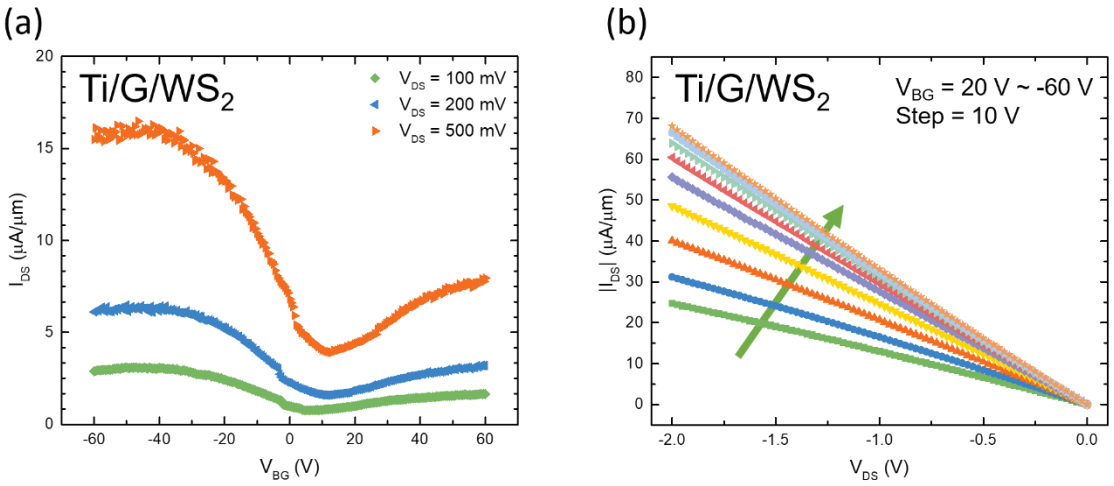

Figure 5-5 Electrical transport measurements of a Ti-G-WS_2 FET with O_2 plasma RIE time of 7 seconds. (a) Transfer curves as V_{DS} changes from 100 mV to 500 mV. (b) Output curves while the V_{BG} varies from 20 V to −60 V with a step of 10 V.

5.5 Electrical Characterization

5.5.1 Transfer Characteristics

Figure 5-6a,b show the typical transfer characteristics ($I_{DS}-V_{BG}$) of representative metal-WS_2 FETs with Au/Cr electrodes ($\Phi_M \approx 4.50$ eV) and Ni electrodes ($\Phi_M \approx 5.15$ eV), respectively. Both Au/Cr-WS_2 FETs and Ni-WS_2 FETs exhibit n-type FET characteristics at a gate bias sweeping from −10 V to 50 V. These clear n-type behaviours are consistent with previous reported WS_2 FETs with metal contacts,[138,150,168,253] which indicates the Fermi level for all of these metals aligned close to the conduction band of WS_2. After inserting a graphene layer between metal and WS_2, the hole current significantly increases. Both Au/Cr-G-WS_2 FETs and Ni-G-WS_2 FETs exhibit p-type FET characteristics in Figure 5-6c,d. With the increase of gate voltage from −50 V to 10 V, the drain-source current decreases due to the reduction of the carrier concentration in graphene-WS_2 heterostructure. Field-effect mobility of the device is extracted from the transfer curve using the following relation,

$$\mu = \frac{dI_{DS}}{dV_{BG}} \times \frac{L}{WC_{ox}V_{DS}} \tag{5-1}$$

where L is the channel length, W is the channel width, C_{ox} is the back-gate capacitance per unit area (115 aF/μm^{-2}), calculated for the 300 nm SiO_2/Si substrate, and $\frac{dI_{DS}}{dV_{BG}}$ is the slope of the transfer characteristic of the device at V_{DS} = 100 mV. The field-effect mobility of Au/Cr-G-WS_2 FETs and Ni-G-WS_2 FETs owns the peak value of 51.6 cm^2/Vs and 4.6 cm^2/Vs, with on/off ratios as high as 10^6 and 10^5, respectively. The average field-effect mobility among all the devices is 38.2 cm^2/Vs for Au/Cr/G contact and 2.1 cm^2/Vs for Ni/G contact. This p-type behaviour has also been observed by other groups using graphene as contacts,[244,248] however, the reason has not been clearly explained yet. To the best of my knowledge, one reason can be attributed to the nature of CVD grown graphene transferred onto SiO_2 substrates. The PMMA-supported transfer process usually results in p-type doping graphene due to the inevitable PMMA residue as well as potentially trapped H_2O and/or O_2 at the interface of graphene and SiO_2.[254] The other reason can be the Fermi level shift of WS_2 toward the valence band because of the oxygen absorption,[169] which could be introduced in the oxygen plasma etching step when defining the graphene areas. The oxygen atoms/molecules adsorbed at the defect sites of WS_2 surface will act as acceptors to trap electrons, and the removal

of electrons from the channel materials will lead to p-doping effect of WS_2. Based on these two reasons, field-effect mobility has been greatly improved owing to the significant increase in the hole current.

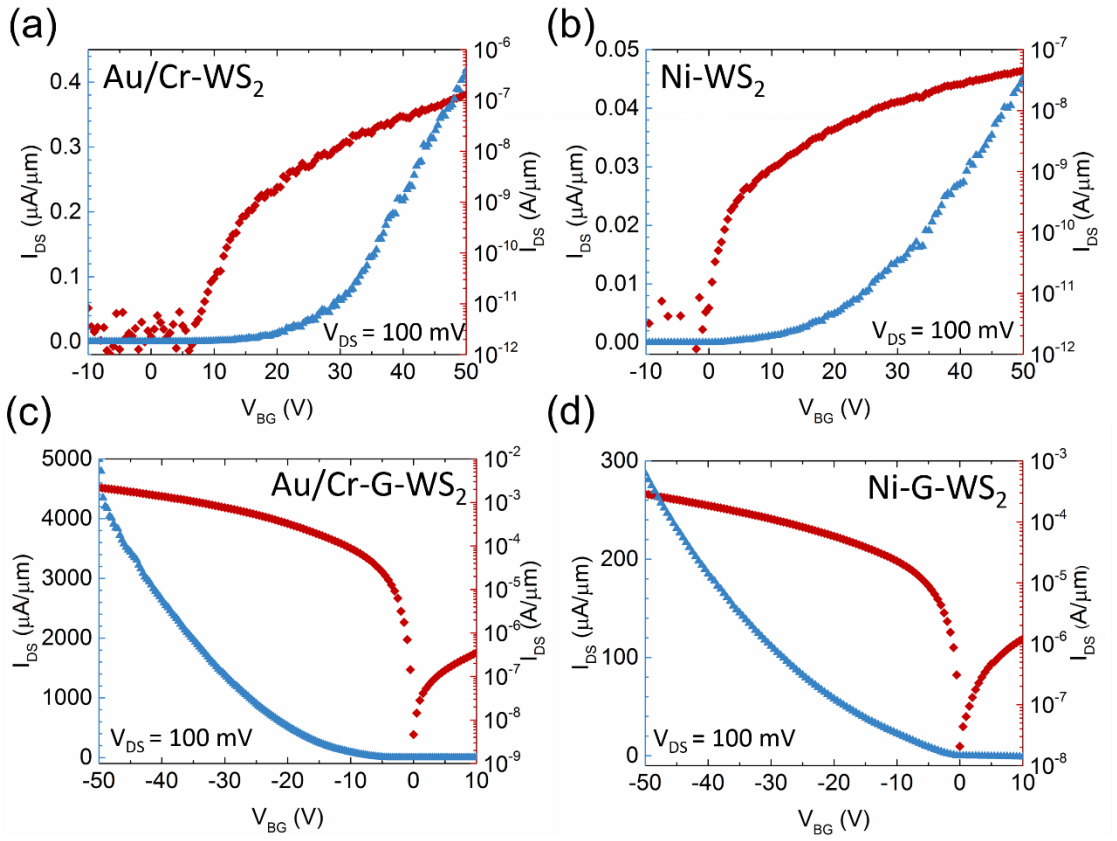

Figure 5-6 Transfer characteristics ($I_{DS} - V_{BG}$) of WS_2 FETs in linear (blue line, left) and log (red line, right) scale with (a) Au/Cr contacts, (b) Ni contacts, (c) Au/Cr-G contacts, and (d) Ni-G contacts. All the devices are measured at drain-source voltage (V_{DS}) of 100 mV. Metal-WS_2 FETs (a-b) show n-type behaviour while metal-G-WS_2 FETs (c-d) exhibit p-type behaviour.

5.5.2 Output Characteristics

The output characteristics ($I_{DS} - V_{DS}$) of corresponding devices are shown in Figure 5-7. The current for both Au/Cr-WS_2 FETs and Ni-WS_2 FETs is nonlinear in the low V_{DS} regime of the output curves, indicating a large Schottky barrier to the conduction band of WS_2 has been formed at the metal/WS_2 interface for devices with either high work function metal (Ni) or low work function metal (Cr). Moreover, the output current with the similar value under the same gate voltage in Figure 5-7a,b demonstrates a strong Fermi level pinning at the metal and WS_2 interface, resulting in very limited modulation of Schottky barrier heights by simply changing metals of different work functions. When introducing a graphene insertion layer between metal

and WS_2, the drain current drastically increases, and total resistance decreases accordingly. Compared with conventional metal-WS_2 FETs, the drain current at the same gate bias of 50 V has been improved by 2 orders of magnitude for Ni-G-WS_2 FETs and by 3 orders of magnitude for Au/Cr-G-WS_2 FETs in Figure 5-7c,d. Without any post-fabrication annealing, the metal-G-WS_2 FETs exhibit linear output characteristics in both cases, and this ohmic behaviour remains when increasing the gate voltage. This phenomenon has been observed in all the devices (over 50 samples), suggesting an ohmic contact has been obtained by inserting graphene layer between metal and WS_2.

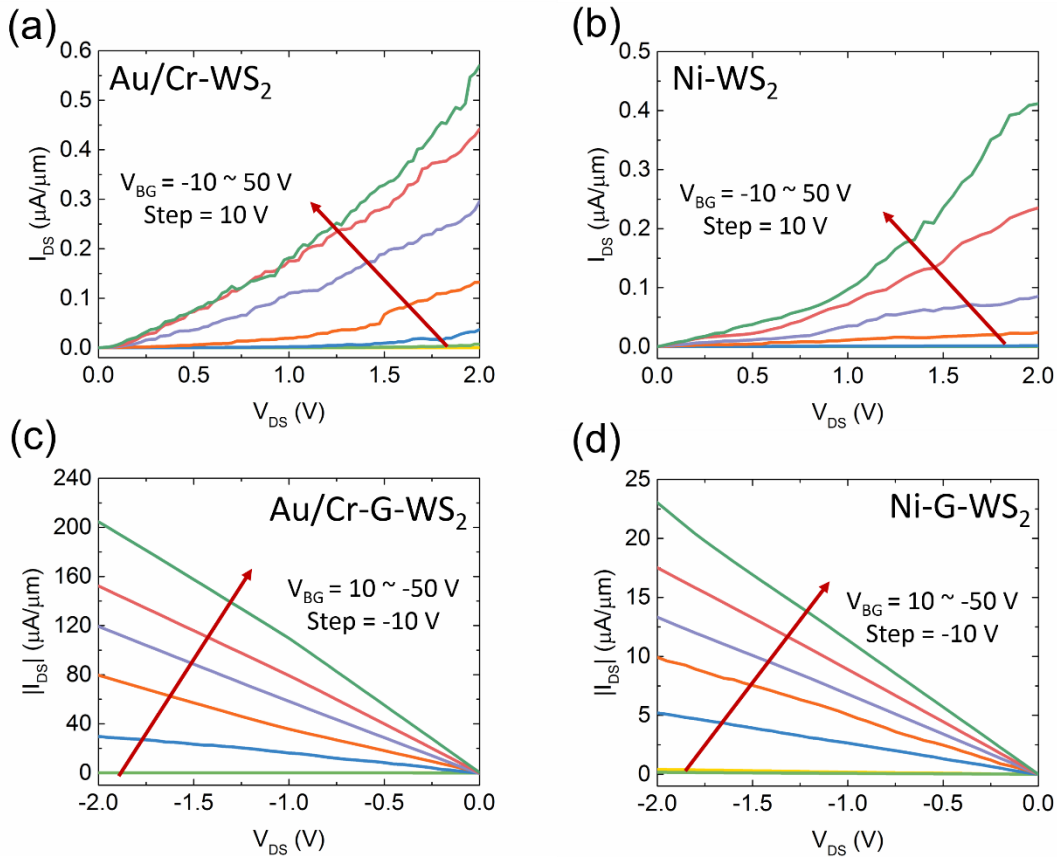

Figure 5-7 Output characteristics ($I_{DS} - V_{DS}$) for different values of the back-gate voltage with (a) Au/Cr contacts, (b) Ni contacts, (c) Au/Cr-G contacts, and (d) Ni-G contacts. The back-gate voltage sweeps from −10 V to 50 V at a step of 10 V for metal-WS_2 FETs, and from 10 V to −50 V at a step of −10 V for metal-G-WS_2 FETs.

5.5.3 Contact Resistance

To better understand the role of graphene insertion layer in increasing the current, the contact resistance can be extracted from the transfer curves. The total resistance is

the sum of the channel resistance (R_{ch}) and S/D contact resistances (R_c), which can be given by:

$$R_{total} = R_{ch} + 2R_c = L / \left(\mu C_{ox} W \left(V_{BG} - V_{TH} \right) \right) + 2R_c = V_{DS} / I_{DS} \quad (5\text{-}2)$$

where V_{TH} is the threshold voltage. At a high $V_{BG} - V_{TH}$, the channel resistance becomes negligible, and the total resistance is dominated by the contact resistance, which is $R_{total} \approx 2R_c$.[139] The contact resistances were calculated from the transfer curves at high V_{BG} (50 V for n-type FETs and −50 V for p-type FETs) and V_{DS} =100 mV. The contact resistance is 378 kΩ·μm and 1107.4 kΩ·μm for WS_2 FETs with Au/Cr and Ni contacts respectively, which are consistent with previous works.[116,167] With graphene insertion layer, the contact resistance can be reduced to 0.0225 kΩ·μm and 0.174 kΩ·μm for Au/Cr-G-WS_2 FETs and Ni-G-WS_2 FETs as shown in Figure 5-8. This method can achieve much smaller contact resistances compared to other methods like using dielectric layer (24 kΩ·μm)[116] or introducing Cl doping (0.7 kΩ·μm)[167].

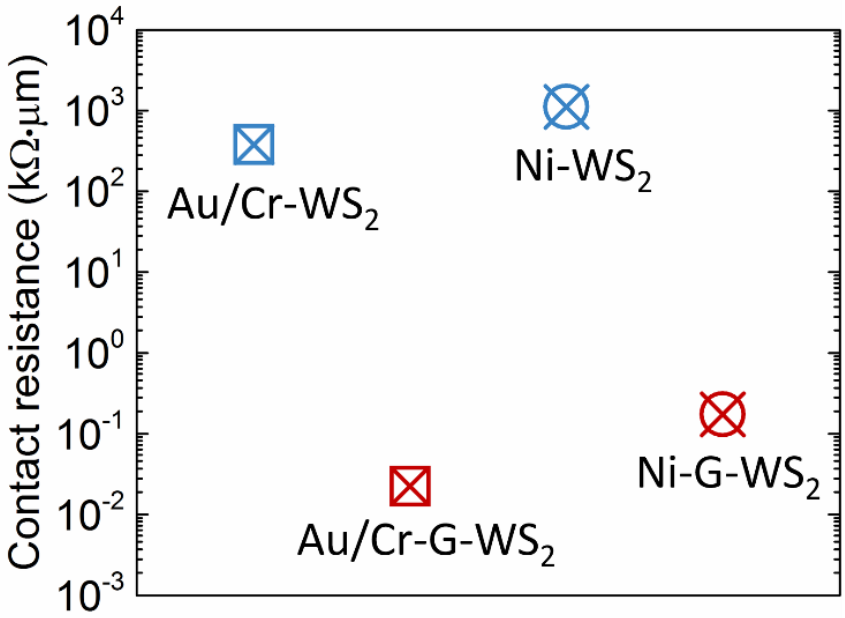

Figure 5-8 Contact resistance for WS_2 FETs with four different contact structures.

5.5.4 Schottky Barrier Height

The effective Schottky barrier heights (Φ_{SB}) which represent the overall electrical behaviour were extracted from transport properties for devices with or without graphene insertion layer. The current injection consists of two components: thermionic emission current and thermally assisted tunnelling current, and the ratio of these two highly depends on the gate bias. At high gate bias (above the flat band voltage, V_{FB}), the tunnelling current is the dominant component of the overall current. Therefore, simply

using the thermionic emission theory to extract the accurate Φ_{SB} will lead to the underestimation of the barrier height, as the basic assumption which validates this theory is that the thermally assisted tunnelling current is negligible.[6] Only when the gate bias is at or below V_{FB}, the contribution from the tunnelling current can be ignored. Here, the accurate Schottky barrier height is extracted at the flat band voltage condition (V_{BG}=V_{FB}) using the thermionic emission equation.[175,176]

$$I_{DS} = AA^{*}T^{2}\exp\left(-\frac{q\Phi_{SB}}{k_{B}T}\right)\left(\exp\left(\frac{qV_{DS}}{k_{B}T}\right)-1\right) \qquad (5\text{-}3)$$

where I_{DS} is the drain-source current, A is the contact area, A^{*} is the Richardson's constant calculated to be 120 $AK^{-2}cm^{-2}$ using $A^{*} = 4\pi qm^{*}k_{B}^{2}/h^{3} = 120(m^{*}/m)$,[175,255] T is the temperature, k_B is the Boltzmann constant, h is the Planck constant, q is the electronic charge, Φ_{SB} is the effective Schottky barrier height, and V_{DS} is the drain-source voltage. By plotting the Φ_{SB} *versus* gate bias, the turning point of the sublinear and linear regime can be extracted as shown in Figure 5-9.

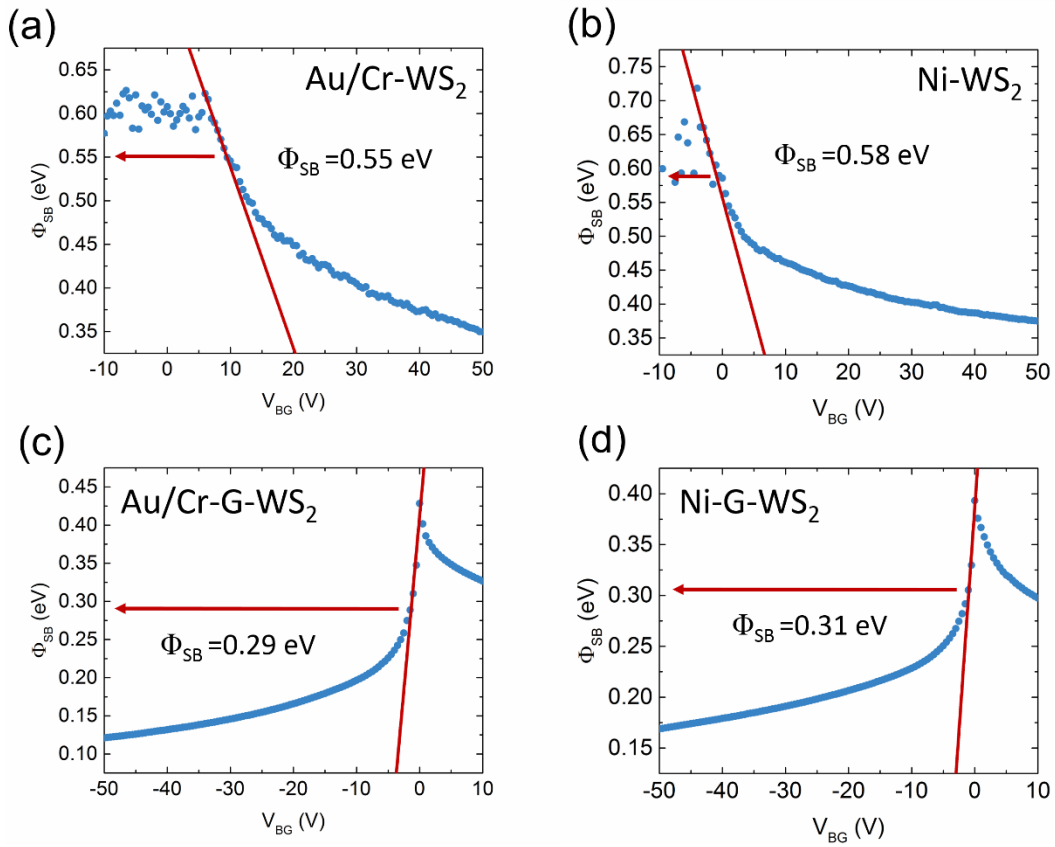

Figure 5-9 Effective Schottky barrier height (Φ_{SB}) as a function of back-gate voltages for (a) Au/Cr contacts, (b) Ni contacts, (c) Au/Cr-G contacts, and (d) Ni-G contacts. The accurate Φ_{SB} at flat band condition is extracted for each situation.

The value at the turning point is the accurate Φ_{SB} when the tunnelling current becomes relevant and V_{FB} is reached. With a graphene insertion layer, the Φ_{SB} decreases from 0.55 eV to 0.29 eV for Au/Cr-G contact, and from 0.58 eV to 0.31 eV for Ni-G contact. Note that further increasing the gate bias ($V_{BG}>V_{FB}$) will result in even smaller Φ_{SB}, as the thermally assisted tunnelling current adds another current component to the overall current. At the gate bias of 50 V, the Φ_{SB} can be further reduced to 0.12 eV (Au/Cr-G contact) and 0.17 eV (Ni-G contact) respectively.

5.6 Different Metal Contacts to WS_2

5.6.1 Ideal Contact and Real Contact

As previously reported in theory[111] and experiments,[116,150,256,257] a strong Fermi level pinning exists at the metal and WS_2 interface, resulting in the Fermi levels for all the metals aligned in the range of mid-gap to conduction band. The calculated Schottky barrier heights based on these experimental results are in the range of 0.3 ~ 0.7 eV when other groups used one or two different metal contacts in their works. To provide a more unambiguous evidence for the strong Fermi level pinning at the metal/WS_2 interface and have a better understanding of this Fermi level pinning effect, a series of experiments using four metals of different work functions was conducted. The channel length for all the devices is 2 μm and the flake thicknesses are in the range of 2 to 5 nm (3 ~ 6 layers). The thickness of the deposited S/D contacts is 50 nm for Ti, Ni and Pd, and 5 nm Cr with 45 nm Au capping layer for Cr/Au stack.

For an ideal metal-semiconductor contact, Φ_{SB} is determined by the difference between the work function of the corresponding metal (Φ_M) and the electron affinity of WS_2 (χ, 3.84 eV for multilayer),[258] which can be expressed as $\Phi_{SB} = \Phi_M - \chi$. For WS_2 of a certain thickness, the bandgap is almost fixed (1.50 eV in my case),[111,177,258] hence the Φ_{SB} can be tuned by varying the metals of different work functions. Metals with low work functions close to the conduction band (E_c), like Ti ($\Phi_M \approx$ 4.33 eV) and Cr ($\Phi_M \approx$ 4.50 eV), and will lead to electron injection, while metals with high work functions close to valence band (E_v), like and Ni ($\Phi_M \approx$ 5.15 eV) and Pd ($\Phi_M \approx$ 5.40 eV), will enable hole injection. Figure 5-10a illustrates the expected line-up of the metal Fermi levels within the electronic bands of WS_2. While in reality, Figure 5-10b displays the actual line-up of the metal Fermi levels according to my experimental results, which

demonstrates that the Fermi levels are pinned in the mid-gap close to the conduction band of WS_2.

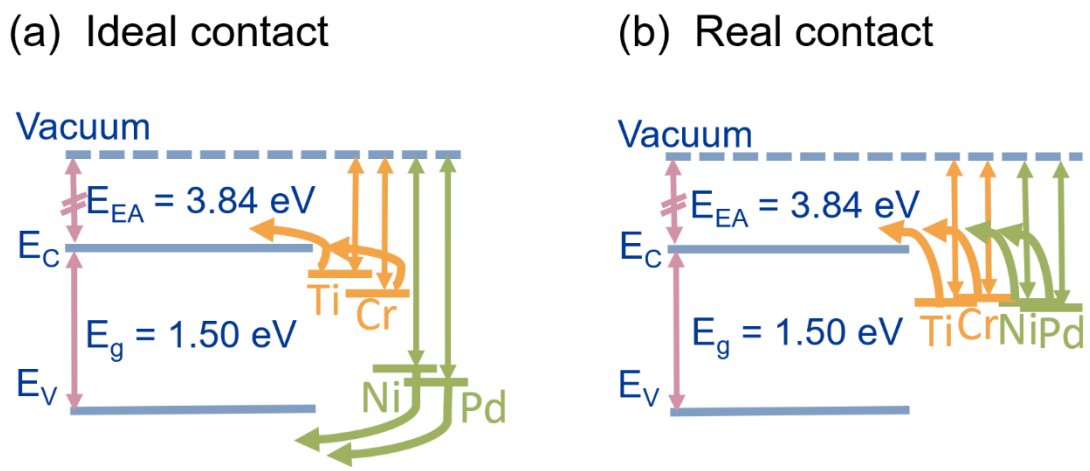

Figure 5-10 Schematic of bandgap diagrams of (a) ideal contact for metal and WS_2 if only considering the difference of the electron affinity of WS_2 and the work function of the corresponding metal; (b) real contact for metal and WS_2 as a strong Fermi level pinning at the interface of metal and WS_2, and the modulation of Schottky barrier heights by metal work function is very limited.

5.6.2 Schottky Barrier Heights of Four Metal Contacts to WS_2

Figure 5-11a shows the transfer characteristics of back-gated WS_2 FETs with Ti, Cr, Ni, and Pd as S/D metal contacts, and different coloured areas represent 4 ~ 5 FETs per metal contacts. These findings show that all of the devices with either low work function metals like Ti and Cr contacts or high work function metals like Ni and Pd contacts exhibit n-type FET behaviours, which implies the Fermi level for all of these metals line-up close to the conduction band of WS_2. Although the Fermi level is not pinned at a certain energy level, it slightly varies in a small region as shown in the overlap area of those transfer curves. Note that the performance of Ti/WS_2 FETs was under expectation for such a low work function metal close to conduction band, while its I_{DS} was even poorer than those with high work function metals. The reason could be the oxidation of the very reactive metal Ti, which affects its conductivity as a metal contact and degrades the overall device performance. Moreover, it should be noted that the ease of charge injection is only one factor that influences the ultimate contact resistance.[8] Experimental results on MoS_2 FETs have demonstrated that the tunnelling injection of Ti contacts is restricted even though the metal work function of Ti is very low, while some lowest contact resistances up to date have been achieved using Cr/Au

or Au contacts.[168,259] Cr was the other low work function metal used for the contact, its capping layer of 45 nm Au protected it from damage and oxidation of the contacts, thus the I_{DS} was relatively high as its metal Fermi level was closer to the conduction band compared to the other two high work function metals (Ni and Pd).

Figure 5-11b summaries the extracted Schottky barrier heights for the different metal contacts as a function of the corresponding metal work functions. It was found the Schottky barrier heights of 0.59, 0.55, 0.58, and 0.60 eV for Ti, Cr, Ni, and Pd, respectively. If ignoring a little higher value of Ti-WS_2 contact that could be caused by oxidization, the extracted slope of $d\Phi_{SB} / d\Phi_M$ among other three metals is in the range of 0.05 ~ 0.08. This clearly indicates the metal/WS_2 interface is strongly affected by Fermi level pinning, and the line-up pinning levels between the mid-gap to the conduction band of WS_2 can also explain why only n-type FET behaviours are observed among four metals' cases even in the situation of using metals with high work functions. Since the Φ_{SB} does not show much dependence with the metal, this strong pinning effect can limit the potential to modulate the Schottky barrier height *via* accordingly changing the metal work functions.

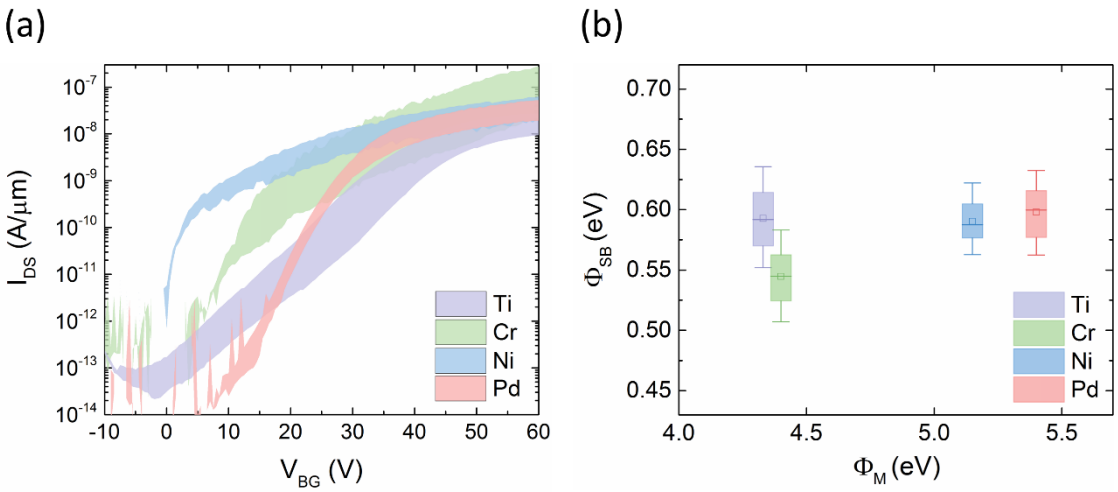

Figure 5-11 (a) Transfer characteristics ($I_{DS} - V_{BG}$) of WS_2 FETs in log scale with Ti, Cr, Ni, and Pd metal contacts. The coloured areas correspond to the transfer curves regions for a number of FETs using the same contact metal. (b) Extracted accurate Φ_{SB} for four metals (Ti, Cr, Ni, and Pd) as a function of different metal work functions.

5.7 Discussion

5.7.1 Doping Graphene with Metal Contacts

The devices with graphene necessarily involve making contacts with metals, thus how graphene is doped by adsorption on metal becomes very important in understanding the device performance. Previous studies reveal that two kinds of adsorbed graphene because of two groups of metals, which are called physisorbed graphene and chemisorbed graphene.[260] Physisorption happens If the metal-graphene interaction is weak, the graphene band structure with the Dirac point can be clearly identified. In contrast, chemisorption is the situation when the binding energy is large, and the graphene band structure is strongly perturbed. Particularly, the characteristic Dirac point at K is destroyed as the graphene p_z states hybridize strongly with the metal d states, resulting in a band structure with a mixed metal-graphene character.

For physisorbed graphene, the Dirac point in graphene band structure is preserved. The work function of a graphene-covered metal W is related to the Fermi level shift, which can be expressed:

$$\Delta E_F = W - W_G \tag{5-4}$$

where W_G is the work function of free-standing graphene. To equilibrate the Fermi levels in the two systems, electrons are transferred between metal and graphene to form an interface dipole and an associated potential step ΔV (Figure 5-12a). Electrons (holes) donated by the metal to graphene result in a shift upward (downward) of the Fermi level with respect to the Dirac point, leading to n-type (p-type) doped graphene. The physisorption doping takes place in Al, Ag, Cu, Au, Cr/Au, and Pt (111).[231,260] However, the bonding of chemisorbed graphene is more complex. The strong metal-graphene bonding interaction results in a considerable dipole that further shifts the metal work functions upon chemisorbed graphene. Current-in-plane (CIP) transport model has been applied to determine a possible measurement to identify a Fermi level shift shown in Figure 5-12b,c. The CIP geometry assumes that the graphene film is partly covers (or is covered by) metal, whereas the rest part is free standing.[260] Equation (5-4) can be applied to all metal electrodes in the CIP geometry. The amount of band bending is given by ΔE_F. Negative and positive ΔE_F correspond to n-type and p-type doping in graphene, respectively. The chemisorbed doping occurs in Ni, Co, Pd (111), and Ti (0001) surfaces.[260] According to previous simulations and experiments, Al, Ag,

Cu, Ni, Co, Pd (111), and Ti (0001) cause n-type doping in graphene while Au, Cr/Au, and Pt (111) end up with p-type doped graphene.[231,260,261]

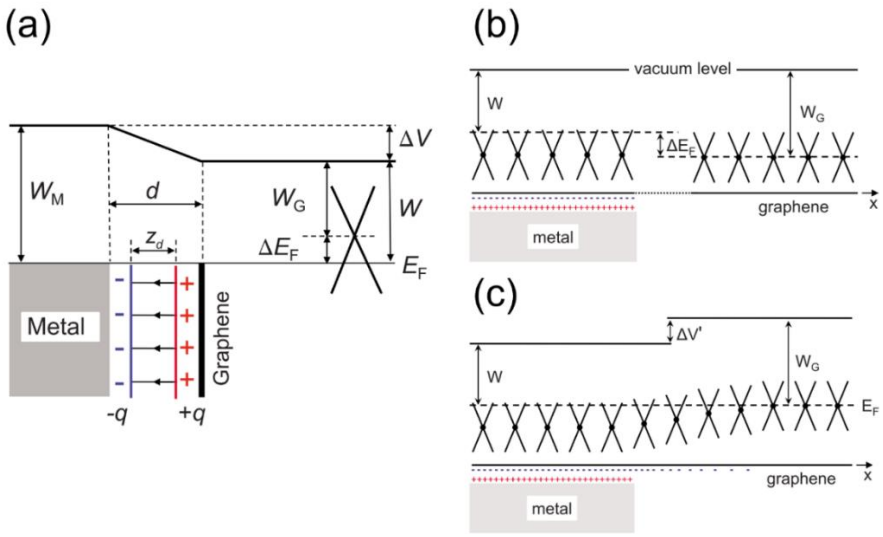

Figure 5-12 Schematic illustrations of the interface dipole and potential step formation at metal-graphene interface in (a) physisorbed graphene and (b-c) chemisorbed graphene. Specifically, (b) depicts the absence of communication between graphene-covered metal and the free-standing graphene, and (c) is the situation after charge transfer to accommodate the Fermi-level difference. *Figures from Khomyakov et al.*[260]

5.7.2 Metal/Graphene Contacts to WS_2

The mechanism behind the increase in current by using metal/graphene contact in WS_2 FETs can be illustrated as the band diagrams shown in Figure 5-13. By introducing monolayer graphene between metal and WS_2, the Fermi level pinning can be modulated. The inserted graphene layer can block the metal wave function penetrating into WS_2 and weaken the metal-WS_2 interaction at the interface, therefore the MIGS is reduced and the Fermi level pinning can be alleviated. Moreover, According to previous studies, the Fermi level of graphene can be shifted away from the Dirac point by chemical doping,[262] external electric fields,[146] and metal contacts.[260] Here, the discussion is based on the metal contact doping theory and effect of the external electric field. As discussed before, the graphene insertion layer is expected to be p-type doped when being contacted with Au/Cr, and n-type doped with Ni,[231,260,261] and the Fermi level shifts relative to the Dirac point are illustrated in Figure 5-13a&c. When no gate voltage is applied, the Φ_{SB} is smaller for the Au/Cr-G contact compared with the Ni-G contact, as its E_F is closer to the valance band. The negative gate voltage will induce holes in

graphene and shifts the Fermi level (E_F) downwards to the valence band as illustrated in Figure 5-13b&d. Specifically, the Fermi level in Ni doped n-type graphene has even been pushed down across the Dirac point by electro-statically doping from the back-gate voltage, where the holes can be injected from graphene to the valence band of WS_2, thus reducing the contact resistance. As a result, the E_F for the Au/Cr-G contact is much closer to the valence band than that of the Ni-G contact at the same negative gate voltage, leading to higher field-effect mobility (51.6 cm^2/Vs) and smaller contact resistance (0.0225 kΩ·μm) of Au/Cr-G-WS_2 FETs as described earlier. This is consistent with the fact that smaller Schottky barrier height can result in better carrier injection and larger current at the metal and semiconductor interface[112] These findings prove that the graphene insertion layer has great capability to form excellent contacts with WS_2 and enhance the device performance.

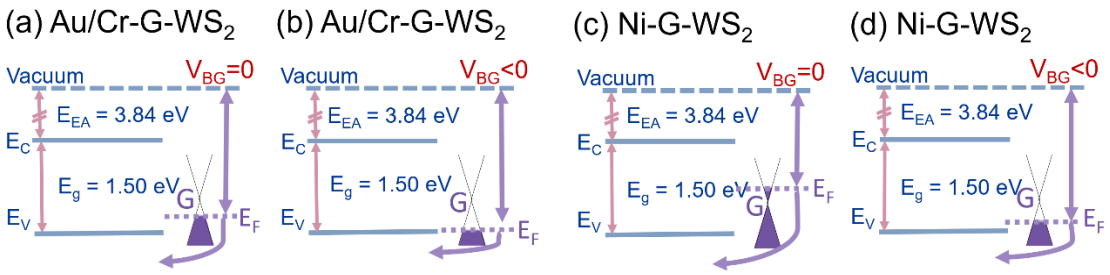

Figure 5-13 Schematic of bandgap diagrams of WS_2 FETs after introducing graphene insertion layer with (a) Au/Cr contact and (c) Ni contact at zero gate bias, and the effective Schottky barrier heights decrease with increasing the negative gate potential for (b) Au/Cr contact and (d) Ni contact.

5.8 Summary

In summary, different metal contacts to WS_2 FETs have been investigated, and the monolayer graphene inserted between the metal and WS_2 has been demonstrated to be an effective approach to reduce the contact resistance. High work function metal (Ni) and low work function metal (Cr/Au) have been first investigated in the metal-graphene hetero-contact structure, and electrical transport measurements show the drain current, on/off ratio, and field-effect mobility have been greatly improved due to the tunable Fermi level of graphene. The on/off ratio as high as 10^6 and a field-effect mobility up to 51.6 cm^2/Vs with a very low contact resistance (0.0225 kΩ·μm) have been achieved for Au/Cr-G-WS_2 FETs at room temperature. The advantage of using metal/graphene hetero-contacts provides a new method for forming low-resistance contacts and boosting performance for TMD electronic and optoelectronic applications.

6 SCHOTTKY BARRIER HEIGHT REDUCTION IN WS_2 FIELD-EFFECT TRANSISTORS BY AN ULTRATHIN DIELECTRIC

In this chapter, an effective approach of reducing the Schottky barrier height at the S/D contacts of WS_2 FETs by inserting an ultrathin Al_2O_3 interfacial layer between the metal and WS_2 has been investigated. Various thicknesses of Al_2O_3 have been used to study the effect of the insulator thickness on the contact resistances. This MIS contact structure demonstrates its great advantage in the Fermi level depinning and the large improvement of on-current and field-effect mobilities in WS_2 FETs. The interface of Al_2O_3 and WS_2 has been investigated to explore the mechanism behind the Schottky barrier height reduction. It was found the blocked MIGS and the creation of dielectric dipoles at the interface can elucidate the shift of the Fermi level. This study provides a novel method to modulate the Schottky barrier height by the optimization of the interfacial material and its thickness.

6.1 Introduction

In Chapter 5, graphene as an insertion layer to reduce the Schottky barrier height at the metal/WS_2 interface has been investigated. The advantages of using a graphene interfacial layer include the effective reduction in contact resistances, the ability to tune the work function of graphene *via* the gate voltage, and the formation of atomically thin 2D devices for future applications. Unfortunately, the integration of graphene with TMDs requires complicated processing steps, such as the optimized synthesis of graphene, extra lithography steps, and complex transfer of materials. All these drawbacks make this method not scalable and applicable for large-scale fabrications. Moreover, the electrical transport behaviours are converted from n-type to p-type due to the inevitable processes introduced in the device fabrication.

Besides the method of inserting graphene layer discussed in Chapter 5, the possibility of reducing the Schottky barrier height while sticking with simplified fabrication processes without changing the electrical properties of WS_2 FETs will be explored. An effective and air-stable approach is to use MIS contact structures by inserting a thin insulator layer between metal and semiconductor. This MIS contact has been previously studied in bulk semiconductors such as Si,[263] Ge,[264] and III-V material,[130,265,266] ZnO[267] and organic material.[268] The commonly inserted insulator include Si_3N_4, Al_2O_3, HfO_2, TiO_2, La_2O_3, and MgO. Recently, this MIS contact has been introduced into TMDs. The insertion of Al_2O_3,[152] TiO_2,[113,152–156] Ta_2O_5,[158] and h-BN[159] have demonstrated their great potential of reducing the Schottky barrier height for metal/MoS_2 contacts. This MIS method has been applied to metal/WS_2 contacts by inserting an ultrathin TiO_2[116] to alleviate the Fermi level pinning.

Despite efforts by several research groups, there is still no thorough understanding of how this MIS contact works in 2D semiconductors. In the bulk semiconductors, the MIGS in the insulator or/and the dielectric dipole generated at the insulator and semiconductor interface have been adopted to explain the reduction in Schottky barrier height. Nevertheless, the applicability of these two explanations in TMDs, the underlying mechanism of how the inserted insulator shifts the pinned Fermi level of WS_2, and the physical origin of dielectric dipoles generated at the interface remain still unclear. The effect of the insulator thickness on the device performance and contact resistances of WS_2 FETs have never been studied yet.

In this chapter, an atomic layer deposited Al_2O_3 inserted between metal and WS_2 interface is demonstrated to be effective to lower the Schottky barrier height as a

depinning layer. The on-current of WS_2 FETs with 1.1 nm Al_2O_3 can be significantly increased by approximate 50 times higher than that of WS_2 FETs without any Al_2O_3. The effect of the Al_2O_3 thickness on the Schottky barrier height and the origin of the dielectric dipole have been investigated to provide deeper insights for the application of MIS contacts to TMDs.

6.2 Device Fabrication

Figure 6-1 schematically depicts the fabrication processes of the back-gated WS_2 FETs with a Al_2O_3 interfacial layer inserted between S/D electrodes and WS_2. As shown in Figure 6-1a, WS_2 flakes were first mechanically exfoliated from a bulk WS_2 crystal (purchased from 2D Semiconductors, Inc.) with scotch tape, subsequently transferred from scotch tape onto a PDMS stamp. Then, the PDMS supported WS_2 flakes were transferred onto a SiO_2 (300 nm)/Si substrate (a heavily doped p-type, 1×1 cm^2), which had been cleaned using acetone/IPA and 1 min O_2 plasma treatment before the transfer. This transfer method can avoid the residues and contamination from the scotch tape and obtained thin WS_2 flakes large enough for the following device fabrication.

ALD technique was used to deposit a Al_2O_3 layer on WS_2 at 200°C in Cambridge Nanotech Savannah S200 ALD system (Figure 6-1b). TMA (purity >98%, Strem Chemicals 93-1360) and H_2O acted as metal precursor and oxidant precursor respectively and were introduced alternatingly into the reaction chamber by 20 sccm of nitrogen flow. The pulse time for TMA and H_2O was 20 ms, and the purge time between pulses was 10 s. The thickness of Al_2O_3 was measured by Gaertner L117 Ellipsometer, and the growth rate was 1.05 angstrom/cycle under the growth condition. By changing the number of ALD cycles from 10 to 20, Al_2O_3 interfacial layers with different thicknesses from 1.1 nm to 2.1 nm were deposited on samples.

EBL was used to define the S/D contacts in Nano Beam nB5 EBL system, followed by a thermal evaporation of Cr/Au (5/45 nm) in the homemade Blue evaporator. The lift-off process took place in acetone and then samples were rinsed in IPA and dried with N_2 to form S/D electrodes (Figure 6-1c). To investigate the effect of Al_2O_3 insertion layers on S/D contacts, devices without any Al_2O_3 layer (bare WS_2) were also prepared to observe the direct contact characteristics of metal on WS_2 using the same fabrication procedure and multilayer WS_2 flakes of similar thicknesses.

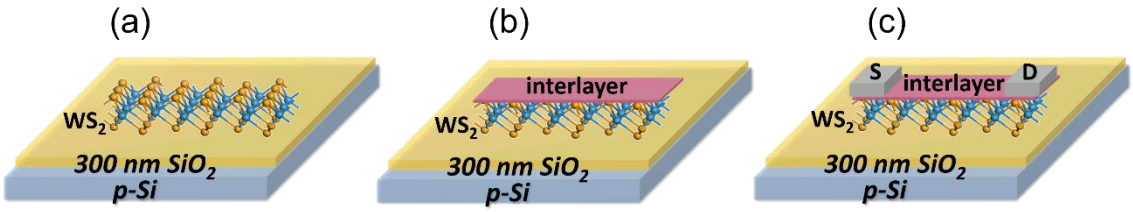

Figure 6-1 Schematic fabrication flows of a WS_2 back-gated FETs with an Al_2O_3 interfacial layer. (a) Mechanical exfoliation of WS_2 flakes onto SiO_2 (300 nm)/Si substrates. (b) ALD Al_2O_3 interlayer with various thicknesses on WS_2 at the temperature of 200°C. (c) Lithography of S/D electrode patterns followed by metal evaporation and lift-off processes.

Figure 6-2 shows the OM images of WS_2 FETs fabricated using the processes described above. The channel length is from 1 um to 3 um and the channel width is from 1 um to 5 um depending on the size and shape of the exfoliated WS_2. Electrical properties of devices were acquired on Keithley 4200-SCS Semiconductor Characterization System connected to a probe station in ambient atmosphere at room temperature.

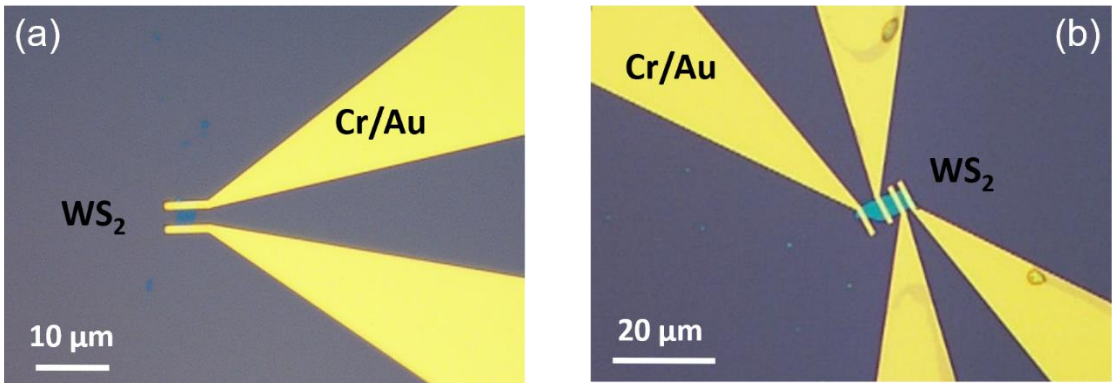

Figure 6-2 OM images of typical WS_2 FETs with a Al_2O_3 interfacial layer between metal and WS_2.

6.3 Material Characterization

6.3.1 Atomic Force Microscopy

The number of the layers for the transferred WS_2 was first identified based on the colour contrast in the OM (Nikon ECLIPSE LV150N) and was further confirmed *via* AFM (Agilent 5500) in a tapping mode under ambient conditions. Figure 6-3b shows the AFM topography of the WS_2 sample (red circle area) in Figure 6-3a. The corresponding height profile (the inset of Figure 6-3b) shows the surface is quite smooth and the thickness is measured to 3 nm, indicating three to four layers of WS_2 flake in

the sample since the thickness of monolayer WS_2 film is in the range of 0.74 nm to 1 nm according to previous papers.[169,177,191]

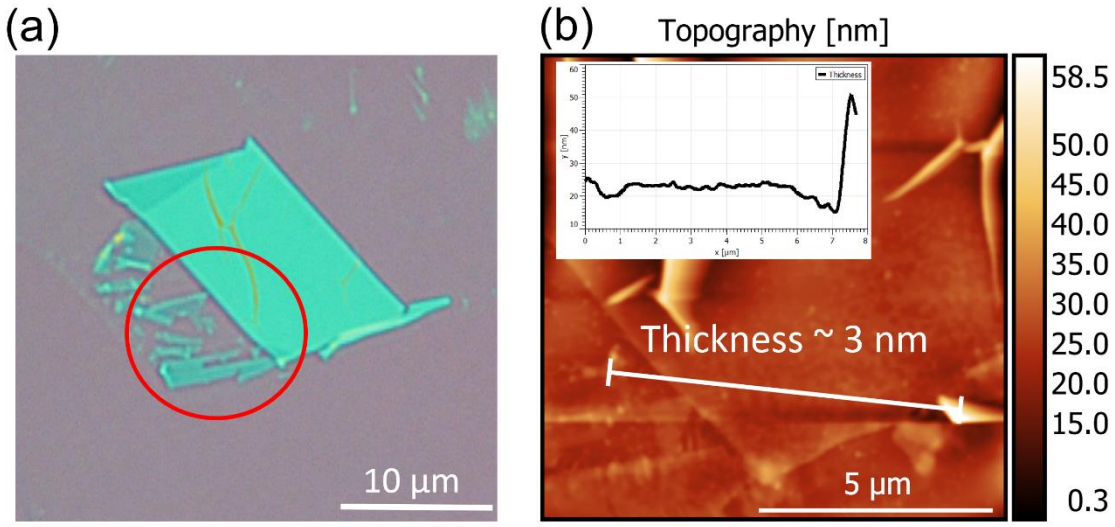

Figure 6-3 (a) OM image of the measured area (red circle) in AFM. (b) AFM image of the topography of the WS_2 sample and the inset is the extracted thickness.

6.3.2 Raman Spectroscopy

The thickness as well as the bandgap information can be further characterized by Raman spectroscopy (Renishaw *InVia* spectrometer) with laser excitation at a wavelength of 532 nm. Figure 6-4a,b show the Raman spectra of WS_2 with different thicknesses. A multi-Lorentzian curve fitting the spectra displays three signature peaks of WS_2, including first-order modes at the Brillouin zone centre ($E^1_{2g}(\Gamma)$ and $A_{1g}(\Gamma)$) and a longitudinal acoustic mode activated by disorder at the M point ($LA(M)$). The OM images of the samples measured by Raman spectroscopy are shown in Figure 6-4c,d accordingly, and the thickness of WS_2 can be determined by the optical contrast between a 2D nanosheet to the substrate.[247] The sample in Figure 6-4c owns more layers than the one in Figure 6-4d, and the identification of the thickness can also be confirmed by the following Raman spectra discussion. The strongest second-order peak, $2LA(M)$ at ~ 356 cm^{-1} and the first-order $A_{1g}(\Gamma)$ at ~ 421 cm^{-1} can be used to determine the thickness of WS_2. The absolute intensity of $2LA(M)$ peak increases with decreasing the number of layers, while the intensity of $A_{1g}(\Gamma)$ displays the opposite behavior.[191] When decreasing the number of layers, the $A_{1g}(\Gamma)$ mode softens, which is in agreement with the decreasing phonon restoring forces in the vibrations due to the weaker

interlayer van der Waals interactions. Moreover, the $A_{1g}(\Gamma)$ mode redshifts (~ 1.87 cm^{-1} in this case) and a slight decrease of $A_{1g}(\Gamma)-E^1_{2g}(\Gamma)$ (from 66.04 cm^{-1} to 64.17 cm^{-1}) is observed with the decrease of the WS_2 thickness, which is consistent with previous studies.[191,269] As predicted theoretically[270] and later demonstrated experimentally,[271,272] compressive strain can enhance the band gap while tensile strain can reduce it. The change of strain can be detected as the $E^1_{2g}(\Gamma)$ mode shifts. The $E^1_{2g}(\Gamma)$ exhibits a very subtle shift when decreasing the number of layers, and this phenomenon has been observed in previous studies.[191,269,272] Additionally, the presence of WO_x on the surface of samples is confirmed by the Raman feature at ~ 270 cm^{-1} and ~ 324 cm^{-1},[273] which might result from the passivation of dangling bonds on the fresh exfoliated WS_2 surface. In conclusion, the bandgap stays almost the same among all the samples, and a commonly used experimental value of 1.50 eV[111,177,258] for the bandgap of multilayer WS_2 has been used in the following discussions.

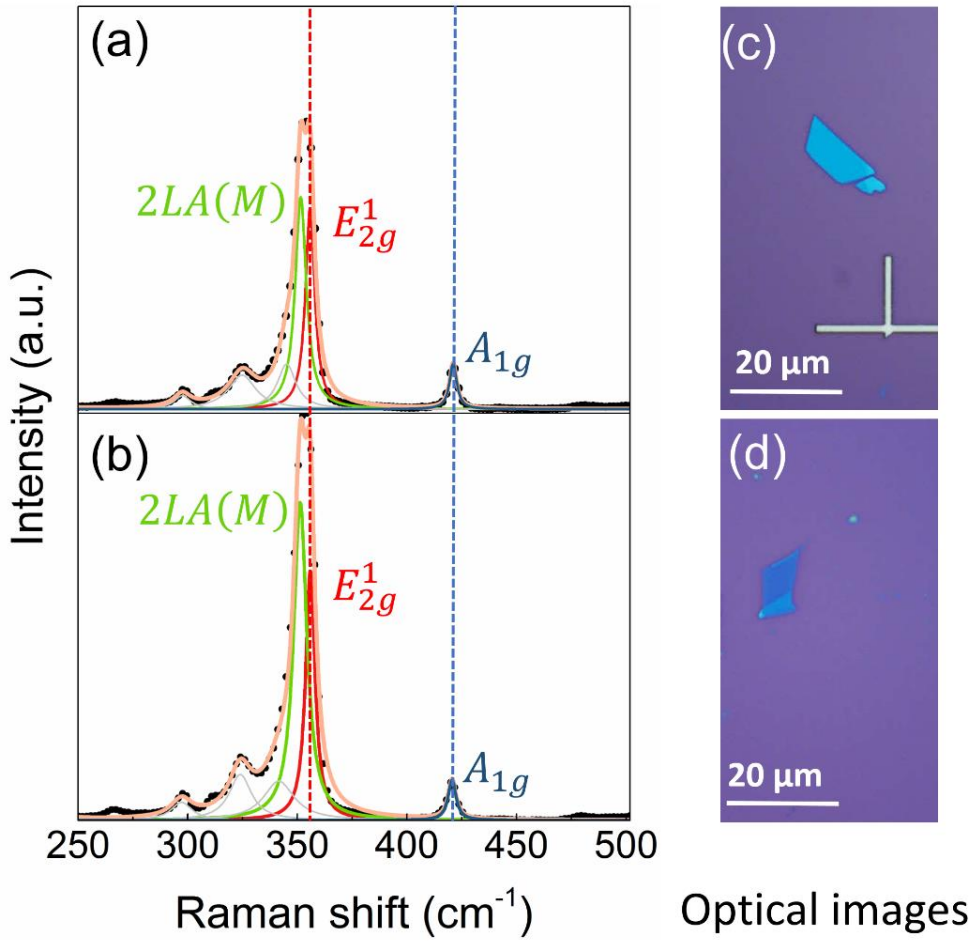

Figure 6-4 (a-b) Raman spectra for WS_2 of different thicknesses, and (c-d) the corresponding OM images of WS_2 flakes.

6.4 Electrical Characterization

6.4.1 Transport Characteristics

Electrical transport properties were measured to demonstrate the effectiveness of Al_2O_3 insertion layers to improve the device performance. Figure 6-5a shows the output curves ($I_{DS} - V_{DS}$) of representative WS_2 FETs with 1.1 nm Al_2O_3, 2.1 nm Al_2O_3, and a control group of WS_2 FETs without Al_2O_3. Without any interfacial layer, a low drain current and a large contact resistance were observed (brown lines). By increasing the thickness of Al_2O_3 to 1.1 nm, the drain current drastically increased (red lines) and then decreased (blue lines) when further increasing the thickness of Al_2O_3 to 2.1 nm. At the gate bias of 70 V and drain-source voltage of 3 V, the insertion of 1.1 nm Al_2O_3 resulted in a significant increase of on-current from 1.25 µA/µm to 28.96 µA/µm, about 22 times higher than that of the WS_2 FET without any Al_2O_3. The 1.1 nm Al_2O_3/WS_2 FET exhibits a good linear and little distortion behaviour with the highest output current among three groups of samples as shown in Figure 6-5b,c, indicating the lowest contact resistance was obtained at the interface.

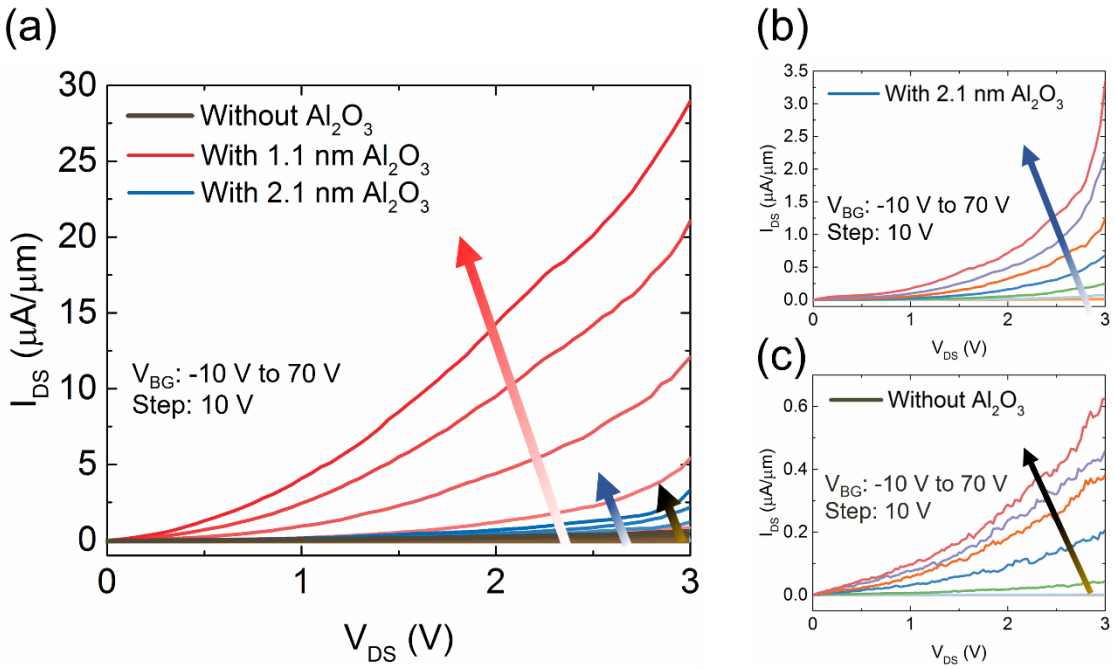

Figure 6-5 (a) Output characteristics ($I_{DS} - V_{DS}$) of 3 typical WS_2 FETs with different Al_2O_3 thicknesses for different values of the back-gate voltage. The back-gate voltage sweeps from −10 V to 70 V at a step of 10 V. (b-c) Zoom-in images of the output curves for WS_2 FETs with 2.1 nm Al_2O_3 and without Al_2O_3.

Figure 6-6 shows the transfer characteristics ($I_{DS} - V_{BG}$) of typical back-gated WS_2 FETs with different thicknesses of Al_2O_3 interfacial layer and the 1.1 nm Al_2O_3/WS_2 FET under different V_{DS} sweeping from 100 mV to 500 mV. All the devices exhibit an enhancement-mode n-type FET behaviour, indicating electron is the majority charge carriers. The average drain current increased by ~ 3 times with 1.1 nm Al_2O_3 and ~ 1 time with 2.1 nm Al_2O_3 interfacial layer. Field-effect mobility of the device (μ_{FET}) is extracted using the expression:

$$\mu_{FET} = \frac{dI_{DS}}{dV_{BG}} \times \frac{L}{WC_{ox}V_{DS}} \tag{6-1}$$

where dI_{DS}/dV_{BG} is the slope of the transfer characteristic of the device measured at V_{DS} =100 mV, L = 2 μm and W = 4 μm are the channel length and width, and C_{ox} is the back-gate capacitance per unit area between the channel and the back-gate (calculated to be 115 aF/μm^{-2} for the 300 nm SiO_2/Si substrate). The peak field-effect mobility of the WS_2 FET with 1.1 nm Al_2O_3 is 5.2 cm^2/Vs with an on/off ratio exceeding 10^6. The increase of drain current was primarily because of a lower barrier to the conduction band due to the depinning effect of Al_2O_3 layer. The passivation of the channel during the ALD process can be attributed to the electron mobility enhancement, as a Al_2O_3 capping layer can suppress Coulomb scattering by dielectric screening.[274]

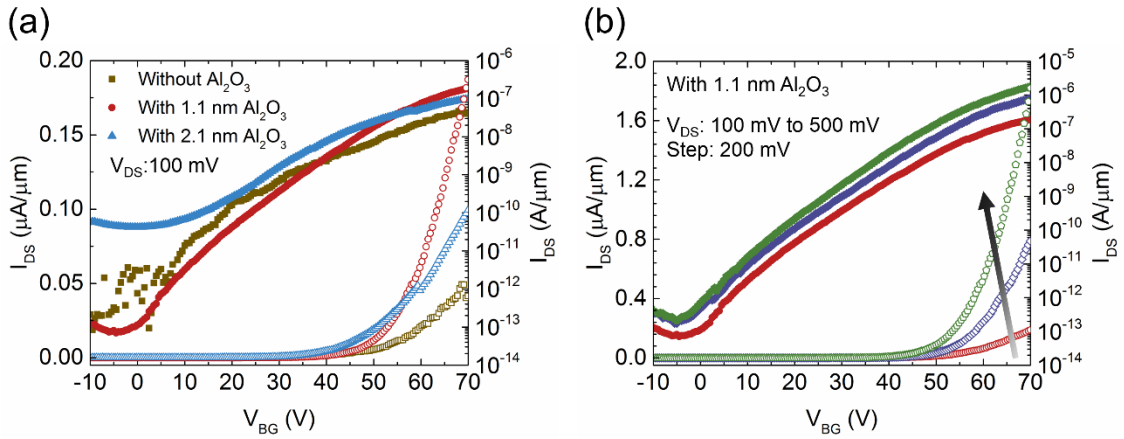

Figure 6-6 (a) Transfer characteristics ($I_{DS} - V_{BG}$) of 3 typical WS_2 FETs with different Al_2O_3 thicknesses at drain-source voltage (V_{DS}) of 100 mV. (b) Transfer characteristics of the WS_2 FET with 1.1 nm Al_2O_3 at different V_{DS} (from 100 mV to 500 mV, step: 200 mV). All the devices exhibit n-type FET behaviors.

The electrical transport properties of WS_2 FETs with two different channel lengths were measured. Figure 6-7 shows the transfer characteristics and output characteristics

of WS_2 FETs with 1.1 nm Al_2O_3 interfacial layer when increasing the channel length from 1 μm to 3 μm, and the OM image of the device is shown in Figure 6-2b. When the channel length is scaling from 3 μm to 2 μm, the increase in drain current indicates the scaling properties in WS_2 FETs. Assuming the carriers follow the diffusive transport in all channel lengths, the saturated drain current exhibits as:

$$I_{DS,sat} = \frac{1}{2}\mu_{FET} C_{ox} \frac{W}{L}\left(V_{BG} - V_{TH}\right)^2 \quad (6\text{-}2)$$

where μ_{FET} is the field-effect mobility of the device, C_{ox} is the back-gate capacitance per unit area, W and L are the channel width and length, V_{BG} and V_{TH} are the gate bias and threshold voltage.[178] Figure 6-7a shows the drain current is inversely proportional to the channel length during in the range of 2 μm ~ 3 μm, which presents a linear characteristic of $I_{DS} - L^{-1}$ relationship as shown in Equation (6-2). However, when the channel length further scaling down to 1 μm, a severe decrease of drain current as well as a sharp drop of on/off ratio down to 10^4 was observed. The decrease of field-effect mobility and nonlinear scaling of drain current are attributed to two reasons. One reason is the contact resistance, which does not scale with channel length but accounts for a substantial proportion of the total resistance compared to the channel resistance especially in FETs with ultrathin body semiconductor and shorter channel length. The other reason is the field-effect mobility shows a descending trend when carriers approach the saturation velocity in shorter channel length devices, and this is consistent with the observation in conventional short channel Si devices.[275] The carrier velocity is proportional to the electric field in a relationship of $v = \mu E$, as a result, the drain current increases with channel length reduction assuming the field-effect mobility remains constant. However, the carrier velocity gets saturated even with the increase of electric field at a very short channel length, leading to the reduction of drain current as well as field-effect mobility as shown in Figure 6-7. Similar phenomenon was observed in MoS_2 FETs,[276] and the conversion point of the channel length in the case of MoS_2 is 500 nm, indicating the short channel effect happens in TMD materials.

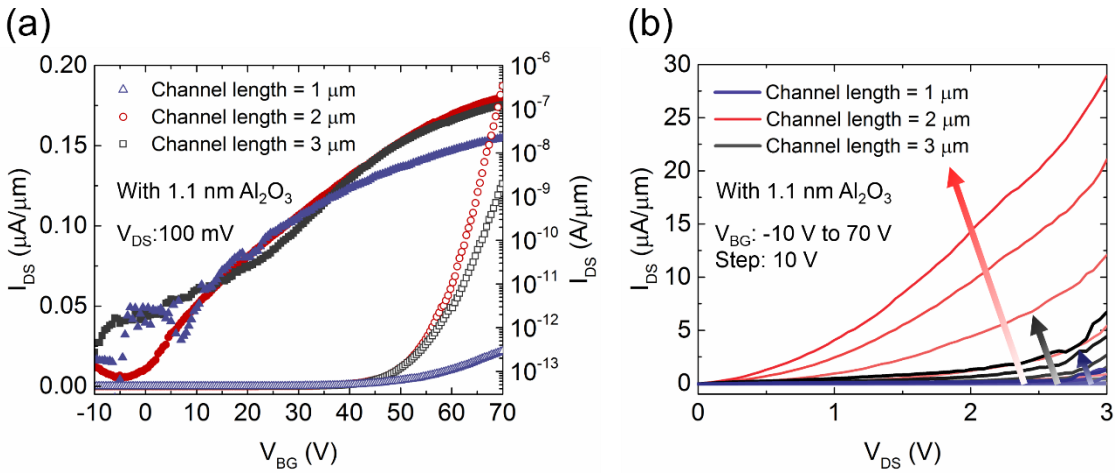

Figure 6-7 (a) Transfer characteristics and output characteristics of WS_2 FETs with 1.1 nm Al_2O_3 of channel lengths from 1 μm to 3 μm.

6.4.2 Contact Resistance

The contact resistance was extracted from the transfer characteristics to analyse the change of the drain current by varying the thickness of Al_2O_3 interfacial layer. The potential drop from the source to the drain is caused by three resistors in series: the S/D contact resistances (R_c) and the channel resistance (R_{ch}). Other than the R_c extraction method used in Chapter 5, here another method to extract R_c from the ratio of two transfer curves ($I_{DS} - V_{BG}$) measured at different drain bias conditions will be introduced.[277] This method is more suitable for the situation when the R_{ch} cannot be ignored. Figure 6-8a,b,c show the total resistances ($R_{total} = V_{DS} / I_{DS}$) for WS_2 FETs with different Al_2O_3 thicknesses under two drain biases. The drain current can be expressed as

$$I_{DS} = \mu_{FET} C_{ox} (W / L)(V_{BG} - V_{TH} - I_{DS} R_c)(V_{DS} - 2 I_{DS} R_c) \tag{6-3}$$

where V_{TH} is the threshold voltage, and R_c can be extracted by varying the drain bias. In this method, assuming R_c is not affected by the drain bias, and a more accurate R_c can be obtained at higher gate overdrives due to the ratio reduction of R_{ch} in the overall resistance. By taking the ratio of two $I_{DS} - V_{BG}$ curves at two drain biases, the following expression can be obtained:

$$\frac{I_{DS1}}{I_{DS2}} = \frac{\mu_{FET1} C_{ox} (W / L)(V_{BG} - V_{TH1} - I_{DS1} R_c)(V_{DS1} - 2 I_{DS1} R_c)}{\mu_{FET2} C_{ox} (W / L)(V_{BG} - V_{TH2} - I_{DS2} R_c)(V_{DS2} - 2 I_{DS2} R_c)} \tag{6-4}$$

The advantage of this approach based on the fact that those two $I_{DS} - V_{BG}$ curves are measured on the same device, which allows us to cancel out C_{ox}, W and L.[277] Note that the field-effect mobility is sensitive to the drain bias *via* the perturbation of the vertical electric field in the channel, and the calculated values of two field-effect mobilities in the devices under two drain biases are different. To simplify the expression using a known term substitution $k = \mu_{FET1} / \mu_{FET2}$ and a cancellation of C_{ox}, W, and L, Equation (6-4) can be rearranged to

$$\frac{I_{DS2} - kI_{DS1}}{2} R_c^{\,2} + \left[k\left(V_{BG} - V_{TH1}\right) - \left(V_{BG} - V_{TH2}\right) + \frac{kV_{DS1} - V_{DS2}}{2} \right] R_c + \left(V_{BG} - V_{TH2}\right) \frac{V_{DS2}}{I_{DS2}} - k\left(V_{BG} - V_{TH1}\right) \frac{V_{DS1}}{I_{DS1}} = 0 \tag{6-5}$$

which is a solvable quadratic equation, yielding R_c as a function of gate overdrive. Since the difference between R_c and R_{total} is the R_{ch}, and the R_{ch} value decreases as the gate overdrive increases, thus a more accurate R_c can be extracted at a higher overdrive.

The contact resistance first decreased from 303 kΩ·μm to 7.1 kΩ·μm when inserting 1.1 nm Al_2O_3 between metal and WS_2 and then increased to 14.6 kΩ·μm with the increase of Al_2O_3 to 2.1 nm. This can be explained by a MIS contact model consisted of two resistances in series: the Schottky barrier resistance (R_{SB}) and the tunnelling resistance (R_T).[158] As shown in Figure 6-8d, when metal directly contacts WS_2, a large Schottky barrier height due to the Fermi level pinning results in a large R_{SB}, which is the major component of the overall contact resistance. With the insertion of ultrathin insulator between metal and WS_2, the Fermi level depinning reduces the Schottky barrier height, thus R_{SB} decreases accordingly. While introducing an insulator additionally adds a small component of R_T to the overall contact resistance when the insulator is very thin. Therefore, R_{SB} is still the dominant resistance and the overall contact resistance decreases with the insertion of 1.1 nm Al_2O_3. By further increasing the insulator, the tunnelling current through the insulator becomes dominant, so R_T accounts for a larger component, thus leading to the increase of the overall contact resistance. Therefore, the trade-offs between R_{SB} and R_T have been first observed in WS_2, and the valley-curve shape is consistent to the earlier reported MoS_2.[158] By varying the thickness of Al_2O_3, the contact resistance can be effectively modulated and there exists an optimal thickness of the insulator in achieving the lowest R_c compared to that of the previous study using a fixed thickness of a dielectric (24 kΩ·μm).[116]

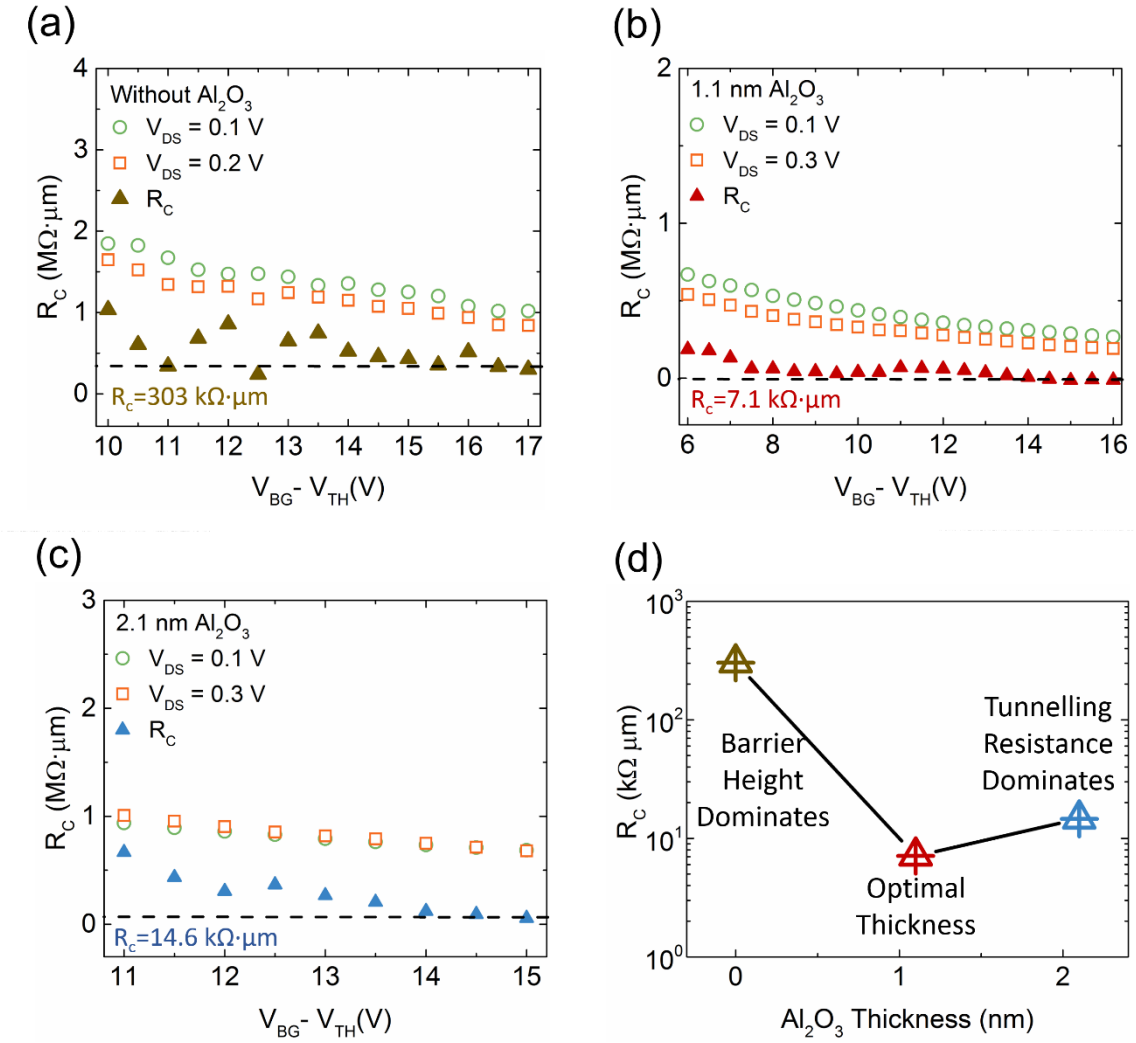

Figure 6-8 Total resistance (R_{total}) of metal/WS_2 FETs under various V_{DS} and their contact resistance (R_c) for (a) without Al_2O_3, (b) with 1.1 nm Al_2O_3, and (c) with 2.1 nm Al_2O_3 as interfacial layers respectively. Open circles and open squares are R_{total} and solid triangles are extracted R_c. (d) R_c as a function of the Al_2O_3 thickness.

The contact resistances of the results in Chapter 5 and Chapter 6 are compared with previous studies of WS_2 FETs using different methods to reduce the contact resistance (Table 6-1). The lowest contact resistance was obtained by using monolayer graphene as the insertion layer, which has been discussed in Chapter 5. This graphene top contact shows better results in reducing the contact resistance compared with the graphene edge contact method. Some doping techniques can be useful to achieve a low contact resistance. However, air instability of chemical doping is a critical issue when using this method. By introducing an ultrathin Al_2O_3 layer between the metal and WS_2 and changing the thickness of Al_2O_3, the method in Chapter 6 can achieve a lower contact resistance compared to the method with a fixed insulator thickness.

Table 6-1 Contact resistance, field-effect mobility and on/off ratio for various WS_2 FETs using different methods to reduce the contact resistance

Ref	Method	Contact resistance (kΩ·μm)	Mobility (cm^2/Vs)	On/off ratio
Work in Chapter 5	Graphene layer	0.02	51.6	4×10^6
Work in Chapter 6	Al_2O_3 layer	7.1	5.2	3×10^6
Ref [167]	Cl doping	0.7	60	4×10^6
Ref [168]	LiF doping	0.9	34.7	10^6
Ref [278]	KI doping	3.75	255	10^8
Ref [116]	TiO_2 layer	24	19	10^4
Ref [138]	Graphene edge contact	30	NA	10^6

6.4.3 Schottky Barrier Height

To understand the mechanism of the R_c reduction, the effective Schottky barrier height is extracted by the thermionic emission equation: [175,176]

$$I_{DS} = AA^*T^2 \exp\left(-\frac{q\Phi_{SB}}{k_BT}\right)\left(\exp\left(\frac{qV_{DS}}{k_BT}\right)-1\right) \quad (6\text{-}6)$$

where I_{DS} is the drain-source current, A is the contact area, A^* is the Richardson's constant calculated to be 120 $AK^{-2}cm^{-2}$ using $A^* = 4\pi qm^*k_B^2/h^3 = 120(m^*/m)$,[175,255] T is the room temperature, k_B is the Boltzmann constant, q is the electronic charge, Φ_{SB} is the effective Schottky barrier height, and V_{DS} is the drain-source voltage. Since both thermionic emission current and thermally assisted tunnelling current attribute to I_{DS} under various gate bias conditions, the Schottky barrier height extracted using the conventional method reflects the overall electrical behavior other than the contact at the S/D. Note that the device operates in the thermionic emission regime when the gate bias is lower than the flat band voltage (V_{FB}), while at high gate bias ($V_{BG} > V_{FB}$), the field emission transport becomes dominant and results in a large amount of tunnelling current, which is only negligible when the gate bias is at or below V_{FB}. The extraction of Φ_{SB} as a function of gate bias is plotted in Figure 6-9 (V_{DS} = 100 mV). For $V_{BG} \leq V_{FB}$, the

effective Φ_{SB} displays a linear behavior to the gate bias. However, as the gate bias further increases above V_{FB}, the tunnelling current mainly accounts for the current transport, and the plot deviates from the linear relation at the flat band voltage condition, where the accurate Schottky barrier height can be extracted. For WS_2 FETs without any Al_2O_3 layer, the extracted Φ_{SB} was found to be 0.55 eV (Figure 6-9a), and the lowest Φ_{SB} was achieved as 0.37 eV for the devices with 1.1 nm Al_2O_3 layer, 48.6% lower than that of the bare metal/WS_2 FETs. As the thickness of Al_2O_3 increased to 2.1 nm, the Φ_{SB} was increased to 0.42 eV due to the large tunnelling barrier added by the thick insulator (Figure 6-9b). Consequently, the Φ_{SB} reduction demonstrates that the insertion of Al_2O_3 can effectively shift the Fermi level from the pinned mid-gap to the level close to the conduction band, thus reducing the Schottky barrier height and increasing drain currents in FETs.

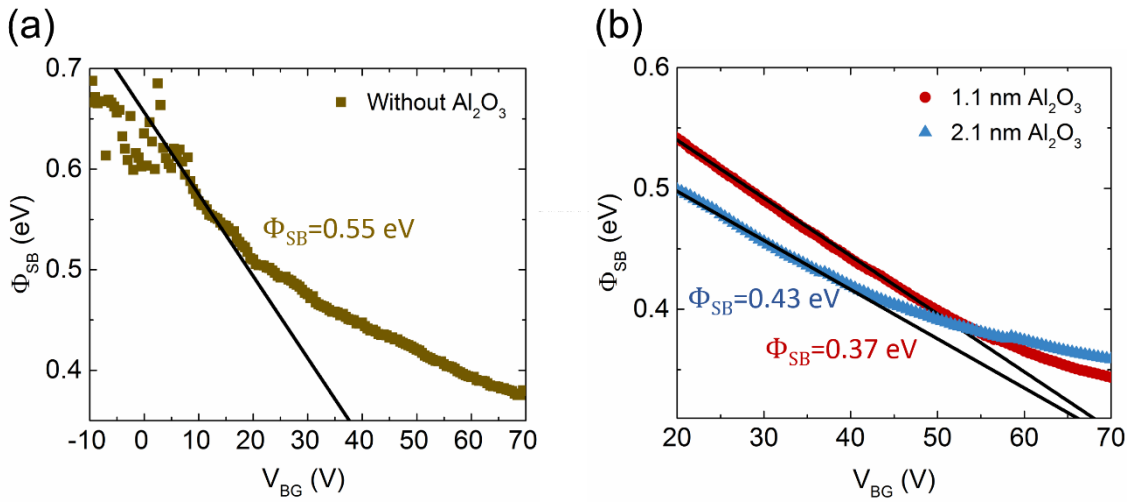

Figure 6-9 Effective Schottky barrier heights (Φ_{SB}) as a function of back-gate voltage (V_{BG}) for metal/WS_2 contacts when the thickness of Al_2O_3 is 0 (brown squares), 1.1 nm (red circles), and 2.1 nm (blue triangles).

6.5 Discussion

The observation of using an ultrathin insulator to reduce the Φ_{SB} is primarily attributed to the unpinning of Fermi level. Despite efforts by some research groups, there is still no complete understanding of how these MIS contacts work in TMD devices. Two possible theories for the observed reduction in Schottky barrier heights have been reported in Si, Ge, and III-V semiconductor MIS contact papers,[130,263,264,266] and the origin of the pinning varies with the chosen Fermi level pinning theory. The two theories considered here are MIGS theory and dipole formation theory. Studying how

these theories explain the MIS contact behaviour will allow us to gain a better understanding of the underlying mechanism.

6.5.1 Metal Induced Gap States Theory

As reviewed in Chapter 2, TMDs follow the MIGS model like those bulk semiconductors. The accurate Φ_{SB} has a linear dependence on the effective metal work function $\Phi_{M.eff}$ instead of the normally referenced metal work function in vacuum Φ_M. The equations are shown below:[109]

$$\begin{aligned} \Phi_{M.eff} &= S\Phi_M + (1-S)E_{CNL} \\ \Phi_{SB} &= \Phi_{M.eff} - \chi_e \end{aligned} \tag{6-7}$$

The insertion of an ultrathin interfacial insulator between metal and semiconductor can block the penetration of the metal electron wave function into the semiconductor, as the metal wave function is attenuated in the insulator prior to the semiconductor. This would result in fewer gap states available to drive $E_{F.\mathrm{int}}$ towards E_{CNL} thus unpinning the surface as Figure 6-10a,b show. In general, the exponential reduction of MIGS and the pinning factor S follow the following expression:[279]

$$\begin{aligned} D_{MIGS}(t) &= D_{MIGS0} \times e^{-2\beta t} \\ S &= \frac{1}{1+\dfrac{q^2 D_{MIGS}(t)(t+\delta)}{\varepsilon_{ins}}} \end{aligned} \tag{6-8}$$

where t is the thickness of the insulator, D_{MIGS0} is the MIGS density when $t=0$, which is the situation of metal and semiconductor contact, β is the rate of decay of the MIGS with the increase of the thickness and is proportional to the bandgap of the insulator, δ is the thickness of the dipole generated at the metal/semiconductor interface without any insulator, ε_{ins} is the dielectric constant of the insulator, and E_{CNL} is the charge neutrality level at which the density of the MIGS and the extent of MIGS decay in the semiconductor δ are minimum, in other word, this is where the Fermi level is pinned (all the energy levels with reference to vacuum). The increase in the thickness of the insulator t causes the reduction of D_{MIGS}, so the pinning factor S will increase accordingly. Owing to the inserted insulator, the higher S means less pinning effect and fewer charges available to drive the Fermi level to the E_{CNL}. This contributes to the reduction of Schottky barrier height from 0.55 eV to 0.37 eV with a 1.1 nm Al_2O_3 interfacial layer in this experiment. When further increasing the thickness of the

insulator, a tunnelling barrier will be introduced and becomes dominant. The conduction band offset (CBO) plays an important role to determine the tunnelling barrier, and the value is expected to be 1.64 eV in this MIS structure (Figure 6-10c) based on the experimental data from previous reports.[106,258,280] The unneglectable CBO in this case accounts for the increase of the Schottky barrier height from 0.37 eV to 0.42 eV by increasing the thickness of Al_2O_3 to 2.1 nm. The ideal insulator should have (1) a sufficient thickness to allow the metal wave function to decay; (2) a large pinning factor to release the Fermi level pinning more effectively; and (3) have the minimum CBO with metal and semiconductor to eliminate the tunnel barrier so that the total barrier height would not have dropped with the increase of the thickness of the insulator.

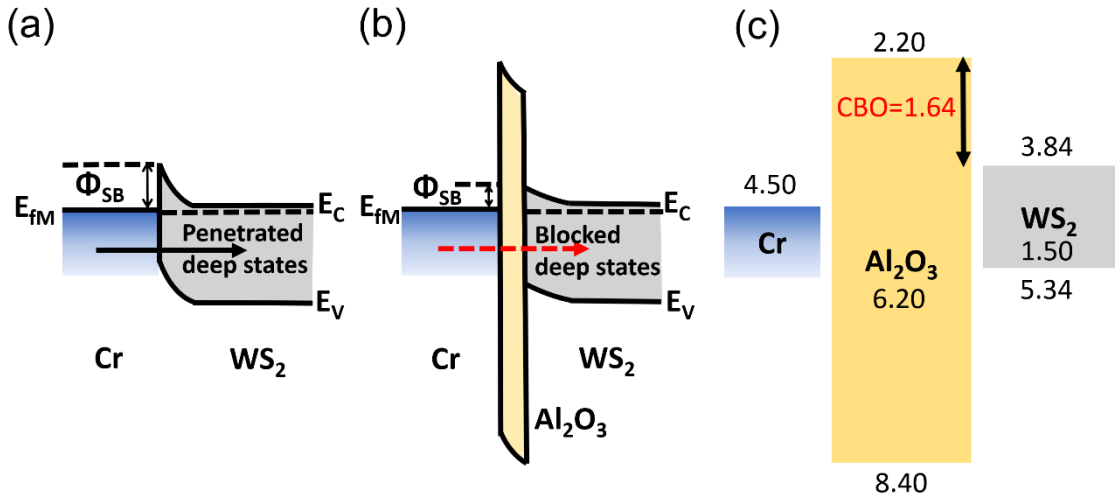

Figure 6-10 Schematic energy band diagrams of (a) a pinned WS_2 Fermi level. A large Schottky barrier height exists at the Cr/WS_2 interface due to the penetration of MIGS; (b) the Schottky barrier height is reduced owing to the insertion of an ultrathin Al_2O_3 layer, which eliminates the penetration of MIGS; and (c) an isolated Cr-Al_2O_3-WS_2 structure, a large Schottky barrier height exists at the metal/WS_2 interface due to the penetration of MIGS. Unit: eV.

6.5.2 Dipole Formation Theory

The difference in the dipole formation theory from the MIGS theory is that the gap states arise from the bond polarization of the chemical bonds at the metal and semiconductor interface, while in MIGS, it is assumed that the distribution of gap states is determined entirely by the semiconductor with no dependence on the metal. To keep the total energy to a minimum, the relaxation and rearrangement of the charge density at the interface take place, generating an interface dipole that pins the Fermi level (Figure

6-11a). In 2D semiconductors, the interface dipole can also be formed as a DFT study demonstrated earlier.[129] They also found the increased separation distance of metal contact from MoS_2 can weaken the modification of the metal work functions and alleviate the interface hybridization leading to fewer gap states at the same time. So, this work provides a theoretical foundation for an insertion of an appropriate buffering material between metal and MoS_2 to unpin the Fermi level. In the case of WS_2, the Fermi level is pinned at the mid-gap, which has been reported theoretically[111] and experimentally.[116] Al_2O_3 was chosen as a buffering layer between metal and WS_2 in my experiment, and a significant increase in the drain current was observed in the output characteristics, implying the Fermi level shifts to the conduction band and contributes to a barrier height reduction for contacts. Therefore, this finding demonstrates an insertion of a buffering layer is effective in the Fermi level unpinning of WS_2 in experiments, consistent with the prediction by theoretical simulations.

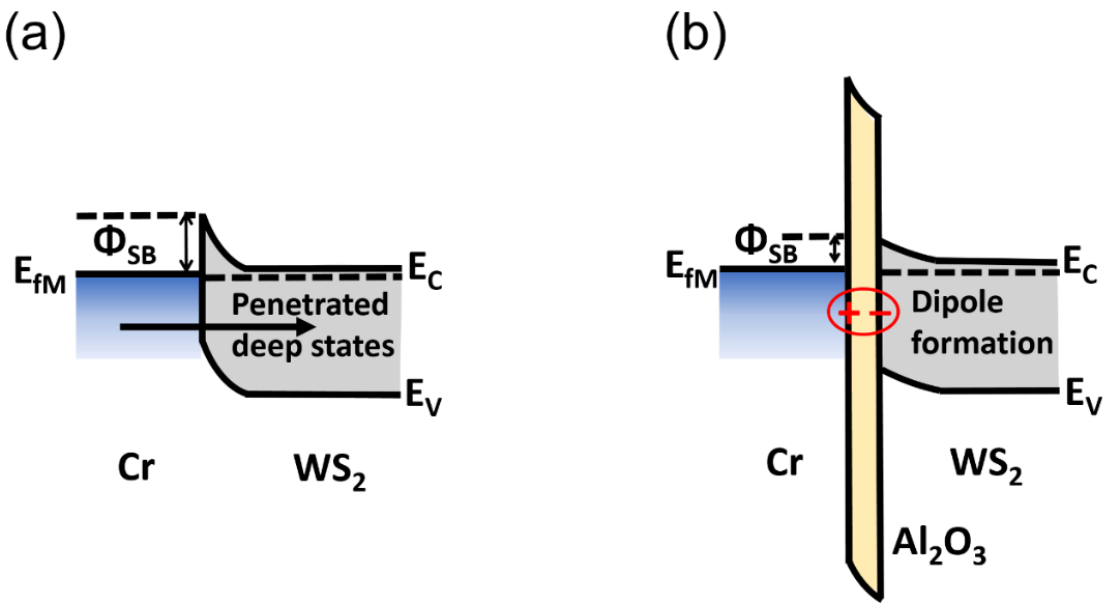

Figure 6-11 Schematic band diagrams: (a) Schottky barrier with a pinned Fermi level, (b) after inserting Al_2O_3 dielectric layer, a dipole is formed at the interface, which can shift the Fermi level and reduce the Schottky barrier height.

It is important to note that all the discussions above are based on assumptions of an ideal interface quality between insulator and semiconductor. However, the interface could not be perfect in real world due to the inevitable oxidation of metals and semiconductors by oxygen in experiments.[279] Therefore, it is very critical and necessary to investigate the dielectric dipole formed in oxides.

Dielectric dipoles at high-κ/SiO_2 were first integrated into Si CMOS gate stacks to scale down the effective oxide thickness while increasing the physical thickness to reduce gate tunnelling leakage. Kita *et al.*[281] found that V_{FB} and V_{TH} shifts were present for a wide range of high-κ dielectrics, and a positive V_{FB} shift was observed when using the high-κ dielectrics that own a lower oxygen density than SiO_2 while those with a higher oxygen density than SiO_2 resulted in a negative V_{FB} shift (Figure 6-12a). The idea of oxygen areal density (σ) comes from the volume difference in the oxide molecules, and the σ difference at the high-κ/SiO_2 interface can drive an equalisation of σ where the oxygen atom moves from the higher σ side to the lower σ side, resulting in a positively charged oxygen vacancy in the higher σ side and a negatively charged centre in the lower σ side. Therefore, a dielectric dipole can be formed at the interface, and shifts the V_{FB} of the MOS capacitor (Figure 6-12b).

Theoretical calculations have verified the V_{FB} shift by high-κ/SiO_2 gate stacks using a detailed DFT study based on atomic models. An interfacial dipole was observed at both the pure HfO_2/SiO_2 interface and the doped HfO_2/SiO_2 interface.[282] It was found interfacial dopants are the main origin of the V_{FB} shift. Specifically, the substitutional La and Sr at the HfO_2:SiO_2 interface create a negative dipole while the substitutional Al, Nb, and Ti form a positive dipole.[282,283] Since the valence band offset (VBO) reflects the internal electrostatic potential across the interface, the VBO shift can indicate the V_{FB} shift in the CMOS gate stack. The calculated VBOs show good consistency with the experimental observations in all cases. Later, a DFT study of the MIS structure (metal/HfO_2/Si) demonstrated the difference of oxygen ion densities exists at the metal/HfO_2 interface and the HfO_2/Si interface.[284] This could cause a net interfacial dipole to alleviate the Fermi level pinning. The dipole formation mechanism obtained from this theoretical calculation shares a very similar idea with Kita's model, that is, the different oxygen ion density at each interface accounts for the creation of diploes. The difference is the interface discussed in Kita's model is between two dielectrics.

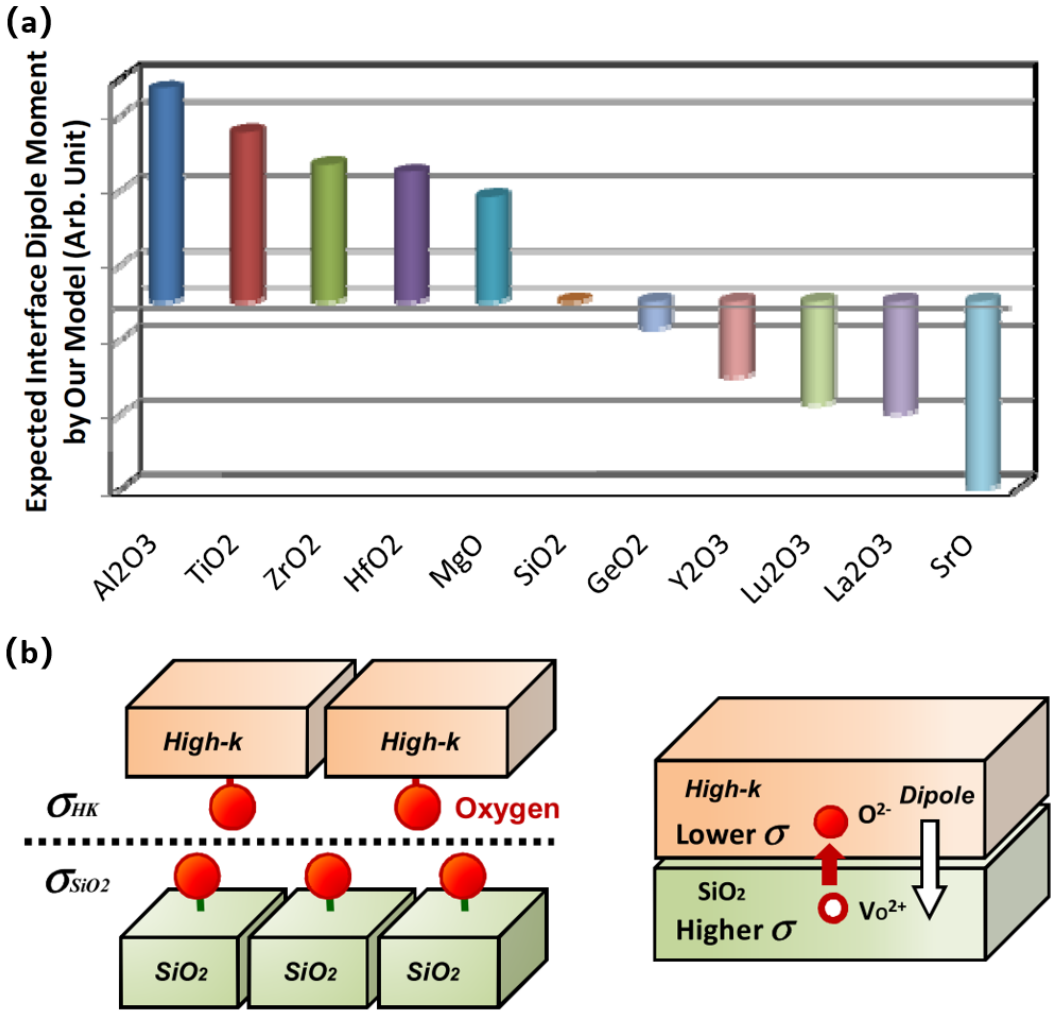

Figure 6-12 (a) Summary of different high-κ materials and their corresponding dipole moment formed at high-κ/SiO_2 interface. The dipole direction to increase V_{FB} is represented as a positive direction. (b) Illustration of the equalization of the oxygen areal density through oxygen transfer at the interface and dipole formation. *Figures from Kita et al.* [281]

To determine the chemical composition of the exfoliated WS_2 films at the contact interface, XPS was conducted. The chemical composition of the transferred WS_2 was analysed by XPS (ULVAC PHI Quantera II) with a monochromatized Al Kα X-ray source scanning a spot size of 50 µm. Figure 6-13 shows the XPS result of the tungsten core levels well fitted by three peaks at binding energies of 32.7 eV, 34.8 eV, and 38 eV, corresponding to $W4f_{7/2}$, $W4f_{5/2}$, and $W5p_{3/2}$ core energy levels respectively.[285] The tungsten in the (4+) valence state indicates the presence of WS_2, which is the dominant component of the material. Note that besides the 4+ valence state in W4f peaks, a small shoulder at binding energy of 35.6 eV (orange line) corresponding to the 6+ valence

state shows the formation of a small amount of WO_3 on the surface of WS_2.[285,286] The oxide might be generated when WS_2 first exposed to air, and can be regarded as the capping layer or native oxide over the WS_2 film. After depositing Al_2O_3, an interface of Al_2O_3 and WO_3 was naturally formed and the density difference of oxygen atoms at the interface creates a dielectric dipole.

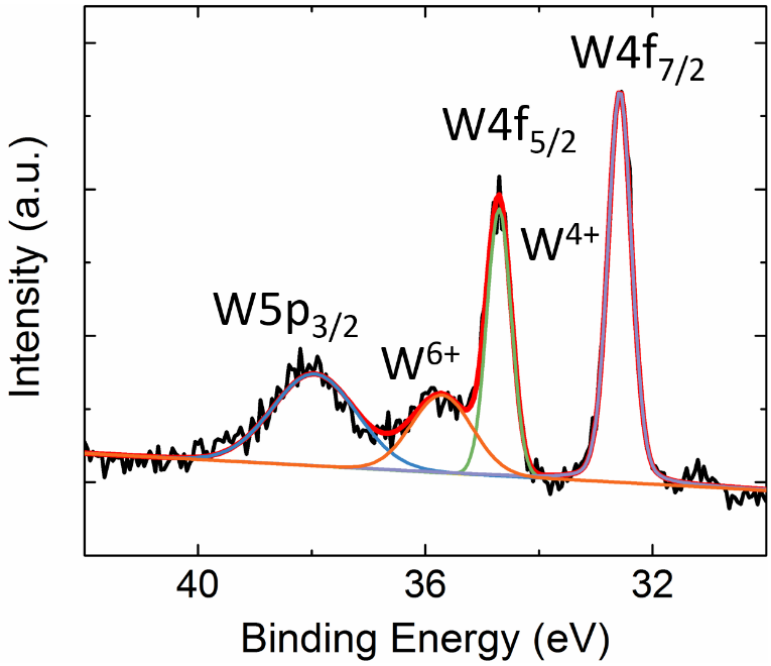

Figure 6-13 XPS spectrum of tungsten core levels, fitted by three peaks including $W4f_{7/2}$ (purple line), $W4f_{5/2}$ (green line) and $W5p_{3/2}$ (blue line).

Based on Kita's model,[281] when two oxides are in contact, there would be a transfer of oxygen from the higher σ oxide to the lower σ oxide, creating a dipole pointing towards the higher σ oxide. σ is defined as the number of oxygen atoms (N) per unit area, and it is approximated by $V_u^{-2/3}$, where V_u is the volume of the structure containing a single oxygen atom ($Al_{2/3}O$ for Al_2O_3 and $W_{1/3}O$ for WO_3). To get V_u, formula volume (V_m) of each oxide is prior calculated by $W_m / (\rho \cdot N_A)$, where W_m is formula weight, ρ is density of oxide, and N_A is Avogadro's constant (6.022140857×10^{23}). The V_u of Al_2O_3 and WO_3 is calculated to be 14.3 Å^3 and 17.9 Å^3, with corresponding σ of 0.171 and 0.146. The calculation details are shown in Equation (6-9) and Table 6-2.

$$\begin{aligned} Molecular\ Weight\ of\ Unit\ Structure = W_u &= \frac{Formula\ Weight}{Number\ of\ Oxygen\ Atoms} = \frac{W_m}{N} \\ Volume\ of\ Unit\ Structure = V_u &= \frac{Unit\ Structure\ Molecular\ Weight}{Density} = \frac{W_u}{\rho \cdot N_A} \\ \sigma &= V_u^{-2/3} \end{aligned} \tag{6-9}$$

Table 6-2 Calculation of σ for Al_2O_3 and WO_3. These values were calculated based on ideal stoichiometry and density values.

Formula Structure	N Number of Oxygen Atoms	W_m Formula Weight (g/mol)	W_u Unit Structure Weight (g/mol)	ρ Density (g/cm^3)	V_m Formula Volume ($Å^3$)	V_u Unit Structure Volume ($Å^3$)	σ ($Å^{-2}$)
Al_2O_3	3	101.94	33.98	3.95	42.85	14.3	0.171
WO_3	3	231.84	77.28	7.16	53.77	17.9	0.146

As shown in Figure 6-14, the σ difference results in a movement of oxygen from the higher-σ material (Al_2O_3) to the lower-σ material (WO_3). Assuming the oxygen transfers in a form of negatively charged ion (O^{2-}), the oxygen movement creates a positively charged oxygen vacancy in Al_2O_3, and negatively charged centre in WO_3, thus forming a positive dielectric dipole pointing towards the higher-σ material. This dielectric dipole can reduce the Schottky barrier height from 0.55 eV to 0.37 eV when using 1.1 nm Al_2O_3 as an insertion layer. This agrees with previous reports[265,266] and paves the way to reduce the Schottky barrier height in metal and 2D semiconductor contacts using the MIS contact structures.

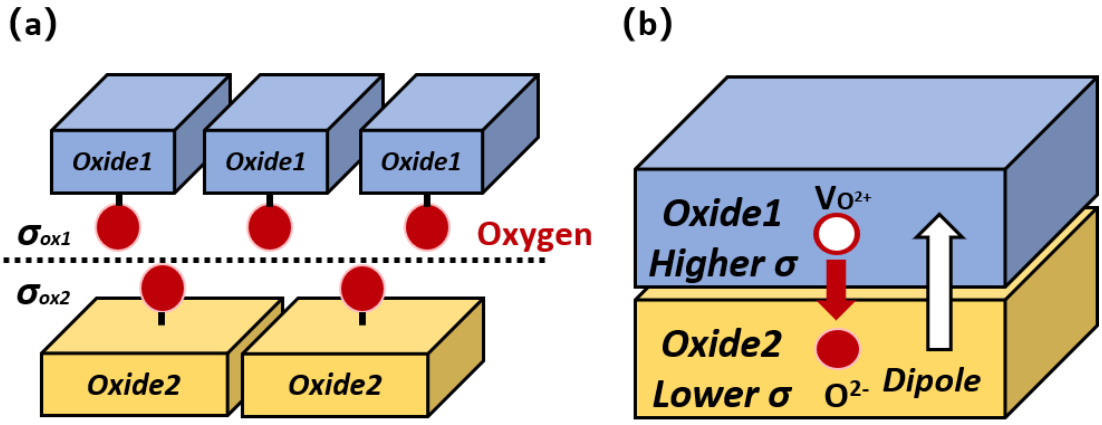

Figure 6-14 Schematic of the transfer of oxygen from the higher σ material to lower σ material, leaving behind a positively charged oxygen vacancy and adding a negatively charged ion in the other side to form the dipole.

6.6 Summary

In summary, an ultrathin Al_2O_3 film inserted between the metal and WS_2 has been demonstrated to work as a depinning layer to shift the Fermi level and reduce the Schottky barrier height at the interface. The underlying mechanism can be explained by the MIGS blocked by the inserted insulator or the dielectric dipole generated at the insulator/native oxide of WS_2 interfaces based on the chosen theory. Furthermore, the effect of different thicknesses of Al_2O_3 layers on the metal and WS_2 contact has been carefully investigated and there exists an optimal thickness of Al_2O_3 in achieving the lowest Schottky barrier height and contact resistance. WS_2 FETs with 1.1 nm Al_2O_3 layer under the S/D metal electrodes as well as the channel capping layer show the largest on-current performance, an improved on/off ratio, and enhanced channel mobilities. This MIS contact structure provides a low-temperature and highly controllable method for reducing the Schottky barrier height at the metal and TMD interface and enables the facile integration of TMD electronics and optoelectronics with the current semiconductor technologies.

7 CONCLUSIONS AND OUTLOOK

The contributions of this thesis include: first, the direct PECVD synthesis of graphene on insulating substrates without any metal catalysts; second, the integration of CVD graphene with the S/D contacts of WS_2 FETs to reduce the Schottky barrier height and achieve low contact resistances, and the investigation of 2D/2D heterojunctions at the interface; third, the application of high-κ dielectrics to WS_2 FETs as an ultrathin interfacial layer between the metal and semiconductor to release the Fermi level pinning as well as the study of 2D/3D heterojunctions at the interface.

In the study of the metal-catalyst-free synthesis of graphene on insulators, the direct synthesis of large-area, low-defect, and N-doped graphene in a microwave PECVD system without any metal catalysts has been achieved. The growth of graphene with two different carbon sources (CH_4 and C_2H_2) has been compared. These results show that replacing CH_4 with C_2H_2 can facilitate the low-temperature growth and reduce the density of defects because C_2H_2 is more active with lower dissociation temperature. Then the effect of NH_3 on the quality of graphene as well as the introduction of nitrogen doping has been studied. Both SEM and Raman results have demonstrated the effective influence of NH_3 on reducing the density of defects and promoting the layer-by-layer growth mode other than 3D nano-wall mode. A uniform and continuous graphene films with the lowest density of defects among all the PECVD growth of graphene can be obtained with the assist from NH_3. Graphene FETs were fabricated using the as-grown graphene, and a typical n-type FET behaviour with a

Dirac point shift to negative gate voltages has been observed, which can confirm the successful introduction of N-doping into graphene. Further investigation of the effect of various insulating substrates on the growth shows that the growth-temperature window and catalytic effect are different among insulators, and the reason could be attributed to their different activation barriers. Al_2O_3 seems to own a lower activation barrier that makes it a promising candidate as a substrate for the low-temperature growth of graphene. As a result, this work offers a systematic study in the optimization and mechanism of the metal-catalyst-free synthesis of graphene on insulators from aspects of carbon sources, etchants like NH_3 and H_2, N-doping, and insulating substrates.

Then this research moved to electronic device aspects using the semiconducting TMDs because the advantages of sizable bandgap and atomic thickness of TMDs enable the booming electronic and optoelectronic applications in 2D world. Fermi level pinning effect has been observed in the experiments of WS_2 FETs with four metals of different work functions (Ti, Cr, Ni, and Pd), and the Fermi levels are demonstrated to be pinned in the mid-gap close to the conduction band of WS_2, resulting in a large contact resistance and Schottky barrier height that could not be modulated *via* the change of metal work functions. Graphene has worked as an insertion layer between the metal and WS_2 to effectively release the Fermi level pinning in this work. High work function metal (Ni) and low work function metal (Au/Cr) have been first investigated in the metal-graphene hetero-contacts to WS_2. By comparing with metal-WS_2 contacts, electrical transport measurements show the drain current, on/off ratio, and field-effect mobility have been greatly improved with the insertion of a monolayer graphene. The mechanism of metal-graphene hetero-contacts has been studied, and the reason could be the metal doping effect on graphene and the tunable Fermi level of graphene by the electric field. Overall, this study investigates the Fermi level pinning effect in WS_2 and provides a new method of integrating graphene with TMDs to form low-resistance contacts for high-performance TMD electronic and optoelectronic applications.

Furthermore, another depinning method of inserting an ultrathin Al_2O_3 interfacial layer between the metal and WS_2 has been investigated. This MIS contact structure was proposed in bulk semiconductor and has demonstrated its capacity as a depinning layer to successfully reduce the contact resistances and the Schottky barrier height in WS_2 in this research. The influence of the different thicknesses of the inserted Al_2O_3 interfacial layer has been first studied in WS_2. This result confirms that an optimal thickness of Al_2O_3 (1.1 nm) exists in the MIS contact to WS_2 in achieving the largest on-current

performance, an improved on/off ratio, and enhanced channel mobilities in FETs. The underlying mechanism for the reduction in the Schottky barrier height can be ascribed to the MIGS blocked by the inserted insulator or the dielectric dipole generated at the insulator/native oxide of WS_2 interfaces based on the chosen theory. Moreover, the conduction band offset of the insulator to WS_2 is crucial to determine the tunnel barrier, and the unneglectable CBO in my case leads to the increase of the Schottky barrier height when further increasing the insulator thickness. Consequently, this MIS contact structure provides a low-temperature, highly controllable, easy to implement method for reducing the Schottky barrier height at the metal and TMD interface and opens up the possibility of the facile integration of TMD applications with existing silicon processing technologies.

Future research can be conducted in the following areas. Firstly, in the study of the direct synthesis of graphene on various insulating substrates, theoretical DFT studies to calculate the activation barriers of various insulators would be beneficial to understand the potential of different insulating substrates for the low-temperature growth of graphene. It would be possible to enlarge the grain sizes, reduce the growth temperature and have a better control of the number of layers if applying the NH_3 recipe into two-step growth method, which can separate the nucleation stage and the growth stage under different temperatures and gas flow rate ratios. Secondly, in the study of graphene-WS_2 FETs, the direct PECVD growth of graphene on WS_2/SiO_2 substrates can tremendously simplify the fabrication processes of WS_2 FETs with the present transferred graphene, and it would be fascinating to fabricate graphene-WS_2 FETs using the direct synthesis of graphene method in Chapter 4. Moreover, the metal-graphene hetero-contacts can be further applied to other semiconductors including bulk materials like Si, Ge, and III-V materials, CNTs and other 2D semiconductors. Thirdly, in the study of inserting an ultrathin dielectric to reduce the contact resistance of WS_2 FETs, it would be very helpful to study the effect of insulators with different CBOs on the tunnelling barrier and finding a dielectric material with zero or negative band offsets would be ideal to obtain barrier-free contacts or even negative-barrier contacts. The controllable modulation of the direction and magnitude of the dielectric dipole can offer the possibility to further reduce the contact resistance and boost the device performance.

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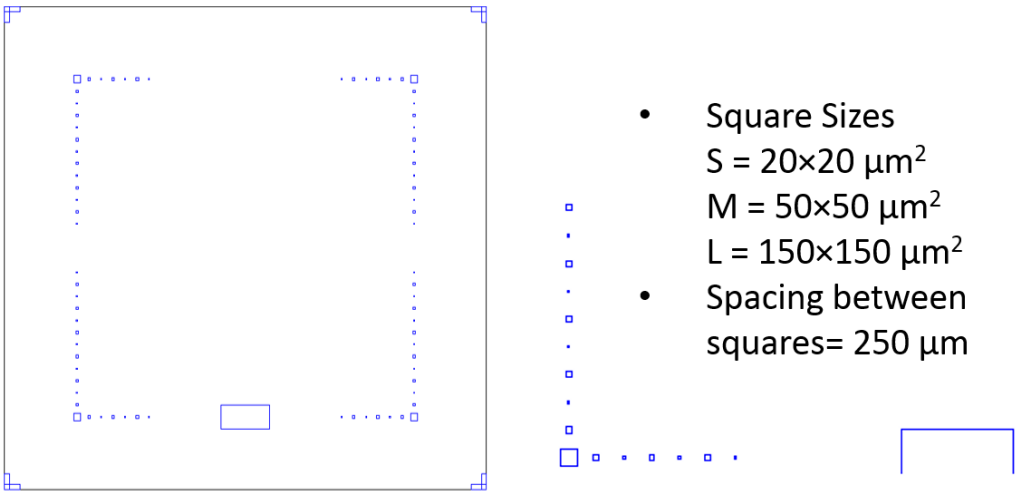
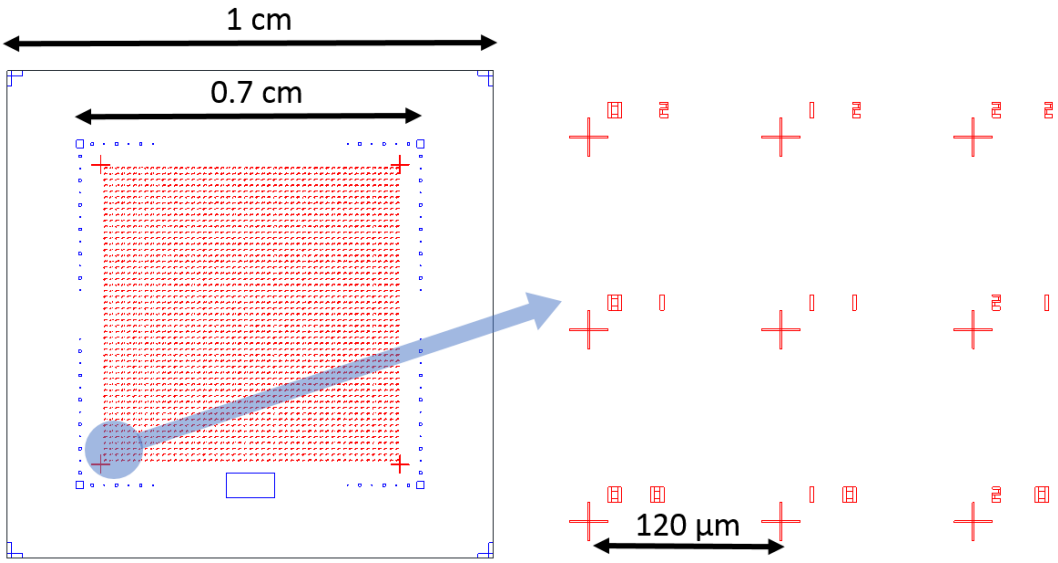
APPENDICES

APPENDIX 1 MASK DESIGN

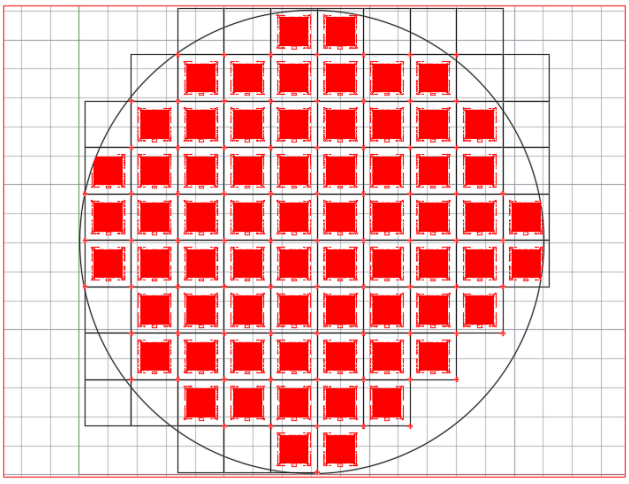
1. Registration Mask



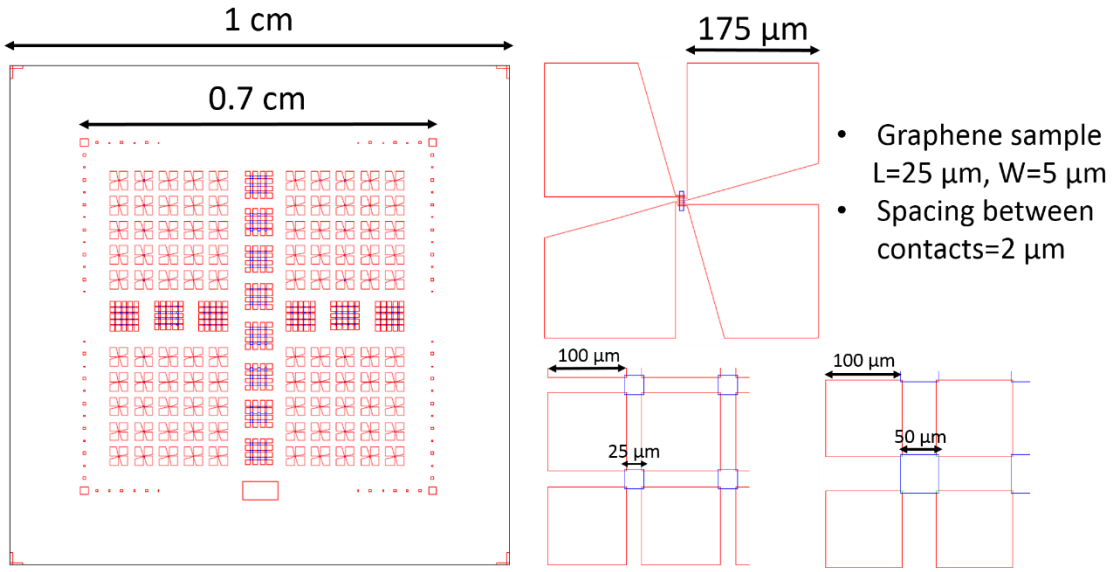
2. Alignment Mask



3. 4-inch Wafer Mask

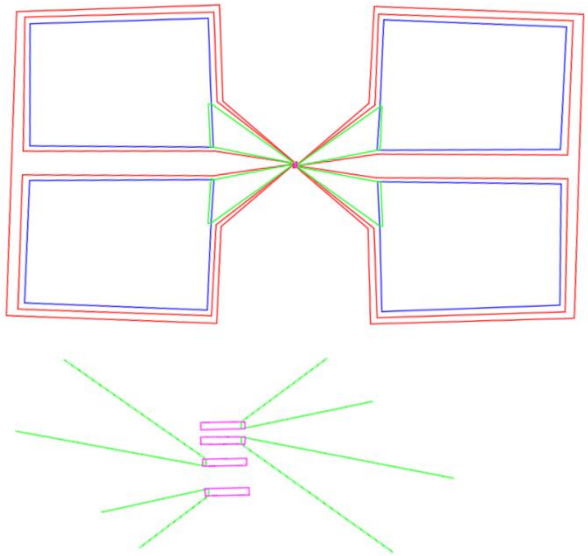


4. Graphene Devices



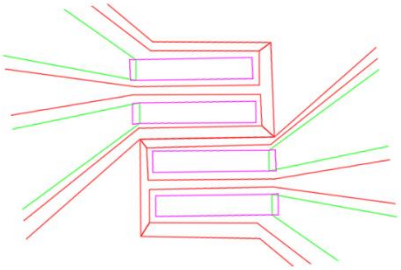
- Graphene sample L=25 µm, W=5 µm
- Spacing between contacts=2 µm

5. WS_2 Back-Gated FETs



- Red: each away graphene
- Purple: feature size: 500 nm ~ 1 µm
- Green: feature size: 1 µm ~ 100 µm
- Blue: feature size: 100 µm ~ 300 µm
- Channel length = 2 µm

- Spacing between contacts = 1 µm, 2 µm, and 3 µm
- Metal contact width = 1 µm

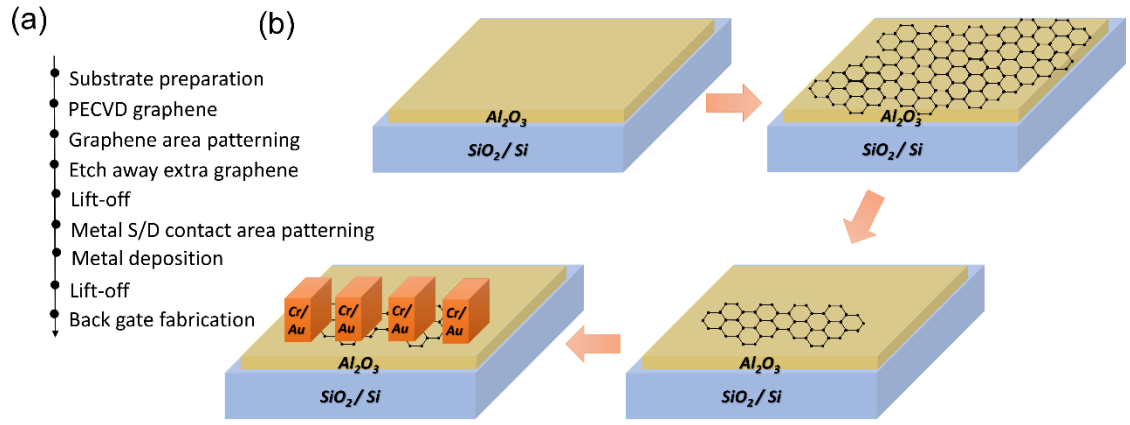


- Spacing between contacts = 2 µm
- Contact width = 2 µm
- Graphene contacts are 100 nm larger at each sides than metal contacts

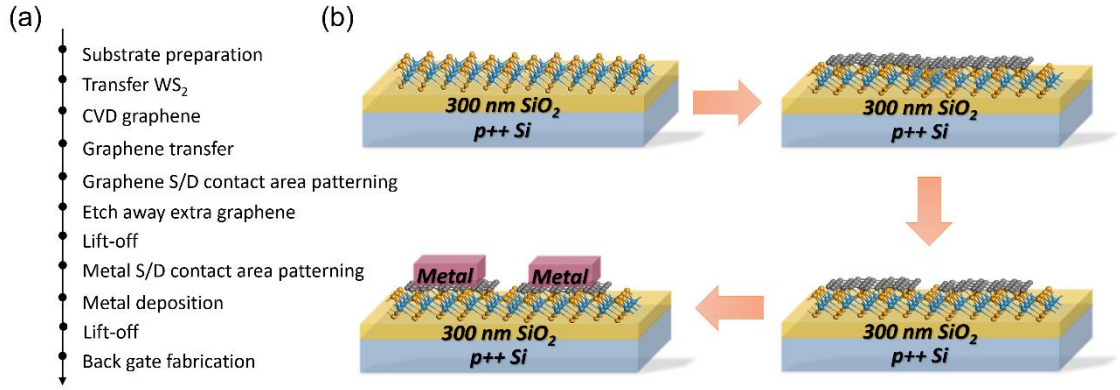
APPENDIX 2 FET FABRICATION

1. Overview

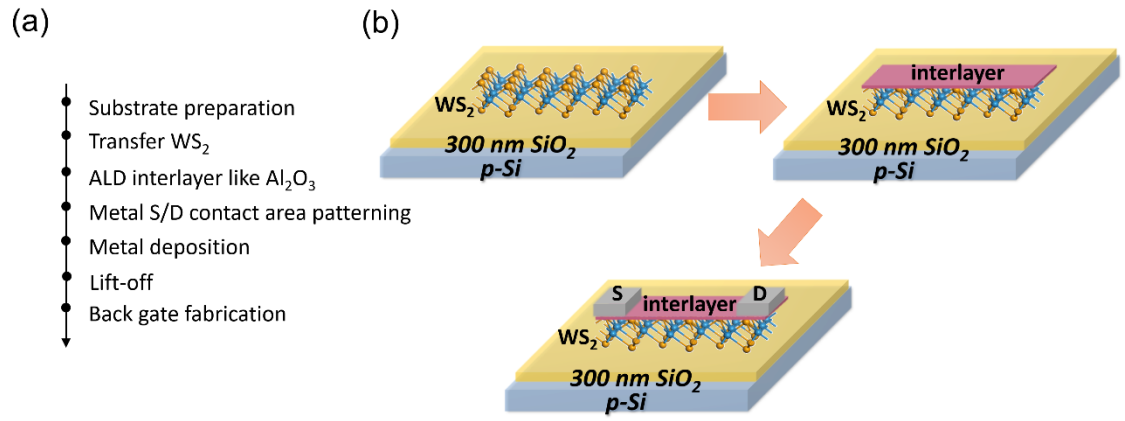
Graphene Device



Metal-Graphene-WS_2 FET



Metal-Al_2O_3-WS_2 FET



2. Process Details
    a. Prepare substrates with marks to locate TMDs
        i. EBL to pattern registration & alignment marks on 4-inch wafers
        ii. Sputter 50 nm Tungsten, lift-off in acetone/ IPA, and dry with N_2
        iii. Dice the wafer into 1×1 cm^2 chips
    b. Transfer TMDs
        i. Pre-treatment of substrate
            1. Clean substrates (300 nm SiO_2/Si) using 5 min acetone and 3 min IPA, dry with N_2
            2. Pre-clean sample with 1 min O_2 plasma
            3. After O_2 plasma treatment, samples must be used within 30 min
        ii. Prepare PDMS
            1. Siloxane base: curing agent = 10:1, and mix with a pipette
            2. Use a pipette to blow away big bubbles or place it in the desiccator for 1 hour to make the surface smooth and flat
            3. Heat it at 70°C on the hot plate for 1 hour or leave it hardened at room temperature for 2 days
        iii. Exfoliation process (with Scotch tape and PDMS)
            1. Take a piece of commercial crystal (2D Semiconductors, Inc.) and place gently on Scotch tape (Tape #1)
            2. Take another piece of Scotch tape (Tape #2) and gently lay this tape on the Tape #1, let it adhere, and press very gently with your fingers. Slowly (1 mm/s) exfoliate tapes from each other. Keep the alpha angel as small as possible and always keep good tension on the tape
            3. Place 1×1 cm^2 PDMS stamp on Tape #2 and press PDMS stamp with a finger, and slowly (1 mm/s) exfoliate PDMS stamp from Tape #2
            4. Place the PDMS stamp on the clean SiO_2/Si substrate, and very slowly (0.5 mm/s) exfoliate PDMS stamp from the substrate

c. Thermal CVD growth of graphene on Cu
    i. Cu electropolishment
        1. Commercial Cu foils (Alfa Aesar, 98.8% purity, 25 μm thickness)
        2. 85% H_3PO_4 solution used as the electrolyte
        3. Voltage: 1.9 V; Time: 30 min
        4. Rinse in IPA and DI water
    ii. Graphene synthsis
        1. 2-inch quartz tube furnace
        2. Heat up to 1030°C at 20°C/min under 1 atm with 400 sccm Ar
        3. Increase Ar flow rate to 4000 sccm to anneal Cu for 5 min
        4. Growth: 3920 sccm Ar, 80 sccm H_2 (2%), and 0.2 ~ 0.8 sccm CH_4 for 10 ~ 80 min
        5. Turn off CH_4 and heating for cooling down
d. Transfer graphene onto WS_2/SiO_2
    i. Graphene: CVD growth on copper foil
    ii. PMMA coating on graphene/Cu
        1. PMMA 950 A4, 4000 rpm, 40s
        2. Dry samples overnight
    iii. RIE to remove backside graphene
        1. O_2 plasma, Philip RIE
        2. Base pressure: 60 mTorr; O_2 pressure ~ 130 mTorr
        3. APC: 200 mTorr; Power: 15 W; Time: 20 s
        4. Cut the edges of graphene/Cu (1mm)
    iv. Cu etching in acid
        1. For one 1×1 cm^2 Cu, use 1.5 g ammonium persulfate ($(NH_4)_2S_2O_8$) and 150 ml DI water
        2. Etch in acid for 4 ~ 5 hours
    v. Transfer onto substrate

1. Use O_2 plasma treated Si to transfer graphene/PMMA from acid to DI water
2. Transfer graphene/PMMA in DI water twice to clean the sample (10 min for each time)
3. Use WS_2/SiO_2 substrates to fish graphene/PMMA in water gently
4. Dry samples overnight

vi. Remove PMMA

1. Rinse in acetone overnight
2. Rinse in IPA for 10 min to remove acetone

vii. Bake at 160°C for 3 hours to improve graphene adhesion to substrates

e. Design masks

i. Use OM to locate TMDs with coordinates

ii. Draw patterns in AutoCAD for EBL

1. Align the OM images with the alignment marks and define the electrode areas
2. The area of the electrode is around 300×200 μm^2 and the channel length is from 1 ~ 3 μm
3. Red line is the pattern of graphene, the other three colour lines are for patterning electrode area. Because the feature size varies (from 1 μm to 300 μm), and different sizes need different electron beam doses in EBL

f. Fabricate graphene contacts

i. Use the registration marks to align the mask with samples

ii. EBL and develop photoresist

1. Photoresist: PMMA 950 A8 for transferred graphene & PECVD graphene
    a. Spin-coating: 5000 rpm, 40s, bake at 120°C for 5 min
    b. Electron beam current: 4.5 nA; dose: 8.5

c. Developing: 7 IPA + 1 DI water for 10 s and dry with N_2

2. Photoresist: UV1116 for PECVD graphene
    a. Spin-coating: 5000 rpm, 40s, bake at 120°C for 2 min
    b. Electron beam current: 4.5 nA; dose: 0.65
    c. Post-bake 120°C for 45 s
    d. Developing: MFD-CD-26 for 30 s, rinse in DI water and dry with N_2

iii. Etch graphene
1. O_2 plasma, Philip RIE
2. Base pressure: 60 mTorr; O_2 pressure ~ 100 mTorr
3. APC: 150 mTorr; Power: 50 W; Time: 10 s

iv. Remove PMMA
1. Rinse in acetone for 10 min
2. Rinse in IPA for 5 min
3. Dry with N_2

g. Fabricate metal electrodes
i. Use the registration marks to align the mask with samples
ii. EBL and develop photoresist
1. Photoresist: PMMA 950 A8
2. Spin-coating: 5000 rpm, 40 s, bake at 120°C for 5 min
3. Electron beam current: 4.5 nA; dose: 8.5, 10.5, 12
    a. Small (purple, 500nm ~ 1 μm) --- dose: 12
    b. Medium (green, 1 ~ 100 μm) --- dose: 10.5
    c. Large (blue, 100 ~ 300 μm) --- dose: 8.5
4. Developing: 7 IPA + 1 DI water for 10 s and dry with N_2

iii. S/D metal deposition
1. Metal sputtering 50 nm Ti or Ni
    a. Pressure pumped down to 1×10^{-5} mbar

b. Growth pressure: 2.5 ~ 3.5×10^{-3} mbar, Ar flow rate: 20 ~ 30 sccm,
c. Pre-sputtering power & sputtering power: 100 W
d. Growth rate: Ti ~ 0.05 nm/s, Ni ~ 0.12 nm/s

2. Thermal evaporation of 50 nm Pd or 5/45 nm Cr/Au
   a. Pressure pumped down to 2×10^{-6} mbar
   b. Growth rate: Pd ~ 0.2 nm/s, Cr ~ 0.1 nm/s, Au ~ 0.2 nm/s

iv. Metal lift-off
   1. Acetone + a drop of IPA, a few minutes to hours
   2. Rinse in IPA and dry with N_2

h. Back-gate fabrication
   i. Scratch the highly doped Si on the back of the sample
   ii. Adhere and fix a Al foil on the microscopy slide
   iii. Adhere and fix the sample with silver conductive adhesion

i. ALD high-κ dielectrics on TMDs
   i. Thermal ALD used to deposit Al_2O_3 by TMA and H_2O
   ii. Growth condition
      1. Carrier gas: 20 sccm N_2; Temperature: 200°C
      2. H_2O pulse for 20 cycles to clean and activate the surface
      3. A single cycle: 20 ms H_2O pulse + 10 s N_2 purge + 20 ms TMA pulse + 10 s N_2 purge
      4. Growth rate: 1.05 angstrom/cycle calculated and measured by ellipsometry